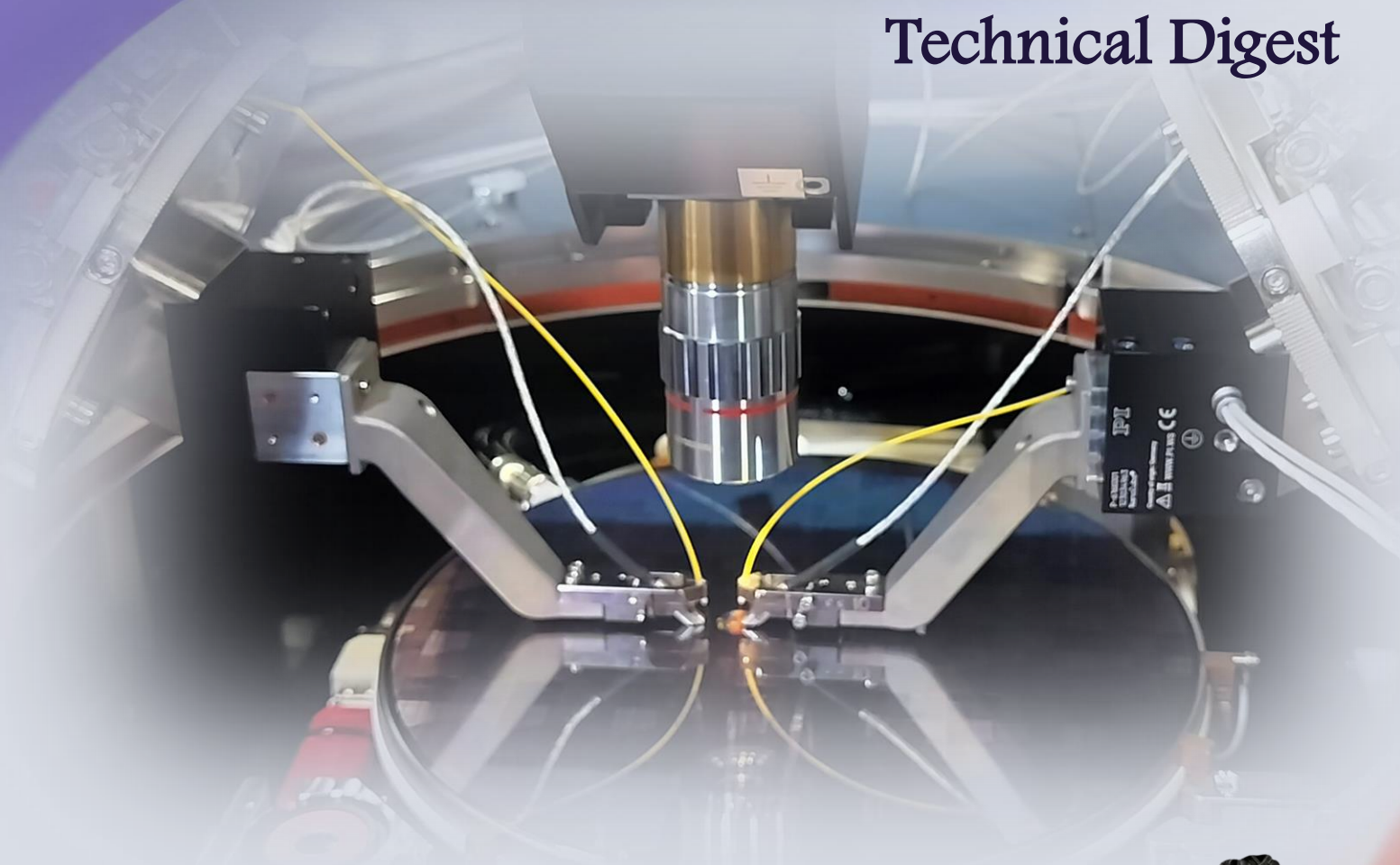
Silicon Photonics
CoE-CPPICS
Technical Digest



Second Edition
20th November 2024

Department of Electrical Engineering
IIT Madras, Chennai – 600 036
Website: https://cppics.iitm.ac.in/

Preface

It has been about an year since the first and inaugural technical digest of our Silicon Photonics CoE-CPPICS was released by the Hon'ble Secretary Shri S. Krisnan, MeitY, Govt. of India. During the last year, we have progressed significantly in terms of demonstrating some landmark experimental results in the domain of quantum photonics and microwave photonics system level applications, contributing towards electronic and photonic design automation (EPDA), developing algorithms for the extraction of silicon photonic wafer-scale manufacturing variabilities, initiating for the development of process design kit (PDK) towards electronic and photonic co-integration, designing DC and high-speed RF PCBs for programmable co-packaged photonic integrated circuits, etc. In addition, our labs have been equipped with a dedicated wafer cleaning station, fully automated silicon photonic wafer scale testing facilities along with a high-performance multichannel quantum photonic measurement system for the last year. All these have been possible because of the collective effort of our entire team CoE-CPPICS and its direct participation and/or in-depth R&D collaboration with multi-national industry partners like Keysight Technologies, Silterra, and izmo Microsystems. A special thanks to my esteemed colleagues Prof. Anjan Chakravorty, Prof. Deleep Nair, Prof. Sankaran Aniruddhan and Prof. Janakiraman Viraraghavan who contributed significantly by training/guiding research scholars and interacting with industry partners on a regular basis by putting their maximum efforts. I also extend my special thanks to MeitY Scientist Dr. SankhaDip Das and R&D Head Smt. Sunita Verma who have been guiding us on a regular basis to execute our committed R&D plan and encouraging us to think beyond, in terms of creating value chain ecosystem for chip-scale manufacturing of photonic integrated circuits and systems to empower digital India.

Once again we would like to put on record that we are enormously grateful to our Director Prof. V. Kamakoti, who has been constantly supporting our R&D by all means. With his far-sight vision and encouragement, we were able to form a very active Industry Advisory Board under the chairmanship of Dr. Mallik Tatipamula (CTO at Ericsson, Silicon Valley, USA), for guiding us to carry out industry relevant R&D activities. The other distinguished members in our CPPICS Industry Advisory Board are industry leaders like Dr. Vivek Raghunathan (Xscape Photonics, USA), Dr. Kishore Kamath (Intel USA), Dr. Steve Johnston (Merck KGaA, Germany), Dr. Prith Banerjee (Ansys USA), Dr. Ravi M. Bhatkal (India/USA Element Solutions), Mr. Narayan Srinivasan (Intel USA), Shri Vijay Janapaty (Broadcom Inc., USA), Shri Vikas Gupta (GlobalFoundries, USA), and Shri Dinanath soni (izmo Microsystems, India). We are also grateful to Dr. Albert Pang (CEO at Silterra Malaysia) who gracefully responded to our invitation and joined as one of the distinguished members of the CPPICS Industry Advisory Board.

Lastly but the most importantly, likewise first edition of technical digest, this second edition is also composed and edited by our research scholars, postdoctoral scientists, and project engineers led by our CTO, Dr. Arnab Goswami. They have organized beautifully their team-wise research contributions which have been carried out during the last one year. Thus we have tried to ensure readers to get a true picture of their intense dedication, team works, passion for scientific research and expressions. I have the fullest appreciation to them for bringing out this 2nd edition of technical digest with in a very short notice period with their greatest level of commitments.

(Bijoy Krishna Das)
Chief Investigator of Silicon Photonics CoE-CPPICS
Professor in Dept. of Electrical Engineering, IIT Madras
Date: 20th November, 2024

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Dr. Albert Pang, CEO at Silterra Malaysia
Shri Dinanath Soni, Executive Director of izmo Microsystems, India

Group Coordinator R&D in Electronics & IT , MeitY, Govt. of India

Sunita Verma
Scientist G & Group Coordinator
R&D in Electronics & IT

भारत सरकार
Government of India
इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी मंत्रालय
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दूरभाष / Tele:

अ॰ स॰ पत्र सं.
D.O.No. GG-11/15/2020-EMCD

दिनांक / Dated 19-11-2024

The Digital India initiative, a flagship program by the Government of India, has played a pivotal role in transforming the nation into a digitally empowered society and knowledge-driven economy. The advancement of silicon photonics and quantum technologies is crucial for India's future in tech-driven innovation.

At IIT Madras, the Ministry of Electronics and Information Technology (MeitY) has supported the establishment of the Centre for Programmable Photonic Integrated Circuit and Systems (CPPICS). Launched in December 2020, this centre is dedicated to designing, manufacturing, and developing applications with Programmable Photonic Integrated Circuit (PPIC) using silicon photonics. This report captures CPPICS's strides in advancing such devices, essential for creating faster and more energy-efficient devices in data processing, digital computing, and next-generation quantum technologies. CPPICS has made significant progress in designing and demonstrating state-of-the-art photonic devices, including Quantum Key Distribution transceivers and programmable photonic architectures. These advancements position us at the forefront of research essential for secure, scalable quantum systems. Key collaborations with industry leaders, such as Keysight Technologies, Silterra, and iZMO Microsystems, have strengthened our ability to transition from research to application. This technology and the associated ecosystem will support Indian sectors in quantum computing, 5G/6G communications, IoT, radar, avionics, and more. CPPICS aligns with the "Atmanirbhar Bharat" vision of Government of India.

We at MeitY truly believe the centre is now ready to compete with the global state-of-the-art which can serve these country's needs decades to come. I extend my best wishes to the center for successfully advancing the technology toward full commercialization and paving the way for PIC manufacturing in India.

Sunita Verma

Digital India
Power To Empower

स्वच्छ भारत
एक कदम स्वच्छता की ओर

ELECTRONICS INDIA
Billion Needs Million Chips

Director of IIT Madras

Indian Institute of Technology Madras
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भारतीय प्रौद्योगिकी संस्थान मद्रास
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प्रो. वी. कामकोटि
Prof. V. Kamakoti
निदेशक
Director

MESSAGE

I am delighted that the R&D team CPPICS is releasing its 2nd Technical Digest showcasing recent progress in the niche areas of CMOS fabrication process compatible silicon photonics technology. As our Country is moving towards building our own capability in the area of Semiconductor Electronics, it is very heartening to see our Institute establish a Centre of Excellence in Silicon Photonics, which is an outcome of extensive R & D pursued over nearly two decades. The substantial seed funding for establishing this state-of-the-art Silicon Photonics Centre of Excellence on Programmable Photonic Circuits and Systems (CPPICS) by the Ministry of Electronics & Information Technology (MeitY), Govt. of India has helped in the **consolidation of indigenously developed silicon photonics technology at IIT Madras. Within a** very short span of time the team has strengthened its research collaboration with industries like Keysight Technologies, Siltera and iZMO Microsystems. My heartiest congratulations to the entire R&D team of CPPICS headed by Prof Bijoy Krishna Das. I am confident that the centre is going to impact significantly, both in the domestic as well as global silicon photonics R & D market in the upcoming years.

V. Kamakoti
(V. Kamakoti)

CTO of Ericsson, Silicon Valley, USA

ERICSSON

November 18, 2024

Industry Advisory Board Chairman – Message

In an era where the convergence of connectivity (5G/6G), compute, control (AI), and sensing shapes the technological landscape, the demand for ultra-fast, energy-efficient, and scalable systems has never been greater. Leading this transformation is the field of Photonic Integrated Circuits (PICs), leveraging the speed and bandwidth of light to overcome traditional system limitations.

Reflecting on the exceptional progress of CPPICS at IIT Madras, I feel immense pride and optimism. By advancing silicon photonics and pioneering programmable architectures, the Centre is setting benchmarks in computing, telecommunications, and sensing, with the potential to revolutionize fields such as 6G, cloud computing, autonomous systems, and manufacturing.

Under the visionary leadership of Prof. Bijoy K. Das, CPPICS has become a hub of excellence. The adoption of a Research, Development, and Manufacturing Model exemplifies a forward-thinking approach, bridging research with impactful applications. Key collaborations, including partnerships with Keysight Technologies and Silterra, highlight the Centre's industry relevance. The upcoming launch of the Electronic-Photonic Design Automation (EPDA) tool, developed with Keysight and integrated into the ADS platform, underscores the ingenuity and dedication of the CPPICS team.

Congratulations to the faculty, students, and staff at CPPICS for your outstanding achievements. Your dedication has established the Centre as a leader in photonic innovation. As Chairman of the Industry Advisory Board, I'm honored to work with an exceptional board to support CPPICS's mission. Together, we're driving transformative innovation in photonics and electronics. Let's continue pushing boundaries and shaping the technologies of tomorrow.

With best wishes for an even brighter year ahead,

Yours sincerely,

Mallikarjun Tatipamula, Ph.D, FREng
Chief Technology Officer, Ericsson Silicon Valley

2755 Augustine Dr., Santa Clara, CA 95054

CEO at SilTerra Malaysia

SILTERRA®

November 19, 2024

Message from Dr Albert Pang Shu Koon, CEO of SilTerra

I am honored to serve as an Industry Advisory Board member for the CoE-CPPICS, a leading R&D organization in the field of silicon photonics, a dynamic field shaping the future of communications, sensing technologies, computing, among other things.

My fervent hope is for CoE-CPPICS to serve as a platform for disseminating cutting-edge research and inspiring innovation in its areas of expertise. By intensifying multidisciplinary collaboration and cross-training between academia and industry, I believe, the impact of meaningful research work in the area of silicon photonics will be further accelerated.

SilTerra is committed to supporting the on-going collaboration with CoE-CPPICS in promoting groundbreaking work that not only advances scientific understanding but also finding viable solutions to address current and future market needs. Thus, let us continue working together to expand the boundaries of innovation.

Best wishes,

Sincerely,

Dr. Albert Pang, Ph.D, Electrical Engineering,
Chief Executive Officer, SilTerra Malaysia Sdn. Bhd.

SilTerra Malaysia Sdn. Bhd. 199501039745 (368948-D)
Lot 8, Phase 2, Kulim Hi-Tech Park, 09090 Kulim, Kedah Darul Aman, MALAYSIA.
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A Member Company DNeX

Executive Director, izmo Microsystems, Bengaluru

izmo

Message

I am delighted that Team COE-CPPICS is releasing it's 2nd Edition of the Technical Digest showcasing the significant progress made in the development of CMOS based silicon photonics technology, achieving lower power consumption and high data throughput.

It has been a year since the Centre for Programmable Photonic Integrated Circuits and Systems at IIT-M got recognised as the Centre for Excellence for Photonics in India by the Ministry of Electronics and Information Technology (MEITY). It was started with a substantial funding by MEITY in the beginning of 2021 with the mission of "Atma Nirbhar Bharat", building the capability within the country in the development and manufacturing of Silicon Photonics Integrated Circuits.

In the advent of artificial intelligence/machine learning and the global demand made on High Power Computing, quantum computing is the need of the hour. Silicon Photonics is critical for rapid data growth and supporting high band width applications. CPPICS R&D team has made significant strides in meeting these technology challenges that would result in lower cost per bit.

All that, in a very short span of time.

Once again, congratulations to Team COE-CPPICS on the remarkable achievements.

Dinanath Soni
Executive Director
izmo Microsystems

izmo Microsystems Private Limited
Ashok Arcade, Plot Nos. 51 & 52, EPIP Industrial Area,
Whitefield, Bangalore- 560066, India

CIN No.: U26101KA2023PTC182295

Major Achievements during Last One Year

(November 2023 - October 2024)

- MoU & SoW signed with SilTerra for advanced level silicon photonics technology development
- MoU & SoW signed with Keysight Technologies for EPDA development to be launched under Keysight ADS platform.
- MoU signed with Hyderabad based startup company amPICQ for joint collaboration and technology transfer
- In-house development of fiber attachment process with grating coupler integrated PICs with quasi-planar couplers (QPC), vertical grooved arrays (VGA) and standard single optical fibers.
- Generation of single photon pairs from microring resonators and demonstration of time-energy entanglement
- In-house demonstration of distributed Bragg reflector based ASE noise removal pump wavelength filters for futuristic chip-scale quantum photonic circuits
- Demonstration of working prototype of a standalone PIC based QRNG module
- Successful in-house demonstration of low-loss silicon nitride waveguides ($\sim$ 0.15 dB/cm) and high-Q microring resonators (Q$\sim 1.7 \times 10^6$)
- Demonstration of SiN-OSP based tunable optoelectronic oscillator (upto 20 GHz) for wireless communication and radar systems.
- First-level demonstration of fully integrated microwave photonic filter with on-chip modulator, optical signal processor and photodetector.
- Proof-of-concept demonstration of programmable photonic integrated circuit (PPIC) based X-band radio over fiber (RoF) receiver link.
- R&D Consortium on Silicon Photonic Enabled Quantum Circuits and Systems (SPEQCS) comprising experts from The Institute of Mathematical Sciences (IMSC), Society for Electronic transaction and security (SETS), izmo Microsystems Bengaluru, and IIT Madras.

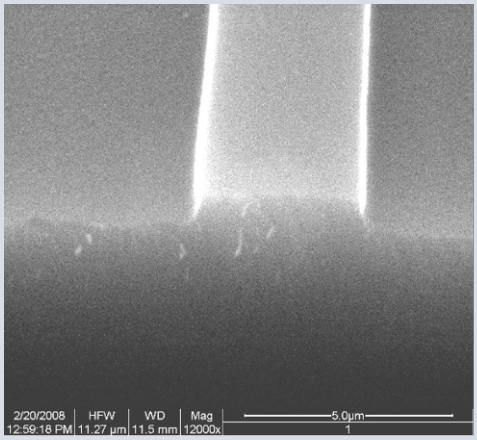
Silicon Photonics @ IIT Madras: Looking Backward

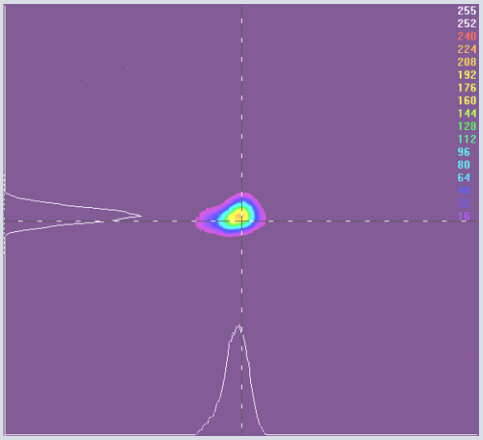
(Aug. 2006 - Dec. 2020)

Though the interests in silicon photonics research among Indian scientists and engineers were noticeable here and there, no planned long-term research goals were set until IIT Madras took the lead to start a silicon photonics research group in 2006. Since then the group at IIT Madras has been actively engaged in novel design, fabrication and characterizations of silicon photonic devices for communication systems and sensor applications. By the end of 2011, various prototype devices were demonstrated by making use of conventional i-line lithography technology (1-μm node) available at IIT Madras. With the availability of nanofabrication facilities at the Centre for NEMS and Nanophotonics (funded by MeitY Govt. of India), the research program was raised to the next higher level – research outcomes have been presented in international conferences, published in peer reviewed journals, and filed as patents as well. The goal of the research group is now set to carry out world class silicon photonics research encompassing novel device designs, CMOS compatible fabrication process optimizations and experimental demonstrations leading towards cost-effective, multi purpose programmable photonic processor chips for microwave and quantum photonic engineering applications. The *Silicon Photonics CoE-CPPICS* is the latest addition in our timeline. Some landmark glimpses of our journey are highlighted below.

Landmark 2007: The first silicon photonic device characterization setup was developed jointly by our first MS Research Scholar Rupesh Navalakhe (jointly guided by Prof. Nandita DasGupta) and first PhD Research Scholar Shantanu Pal in the OCEAN Lab. The optical bench was placed on the top of a coconut coir bed for vibration isolation. All the components used to build this setup was collected from the storage (left over from Prof. Raina) except the IR CCD camera on the extreme right which was bought from the seed grant of Rs. 5 Lakhs from IIT Madras.

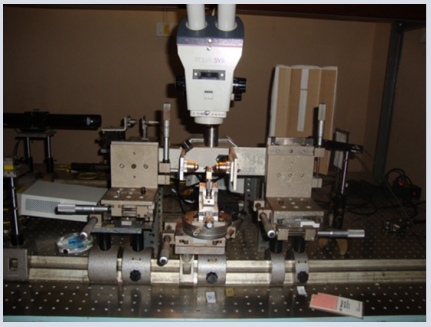
Landmark 2008: The first single-mode waveguide was fabricated at the Microelectronics & MEMS Lab using silicon-on-insulator (SOI) substrate with a device layer thickness of 5 μm. The guided mode was captured by the IR CCD camera which is also shown here.



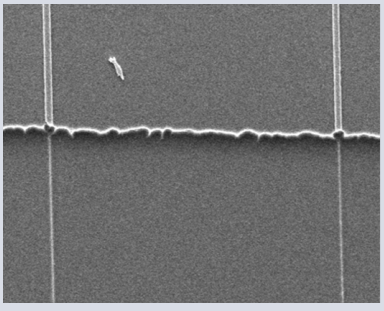


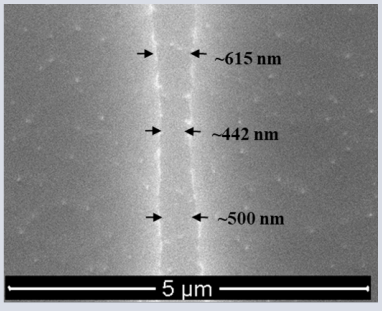
Landmark 2009: The number of students and research scholars increased to a team of eleven and we started calling it as the Integrated Optoelectronics Group. The Integrated Optoelectronics Lab was built in Room No. CSD106.

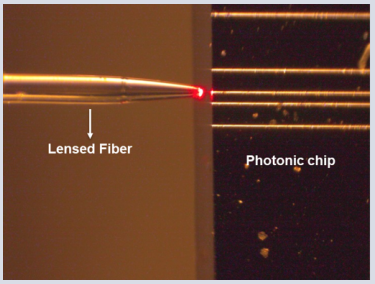
Landmark 2011: Some working silicon photonic prototype devices fabricated at IIT Madras were fiber-pigtailed and packaged in SAMEER, Mumbai. The project was funded by the Department of Information Technology (DIT), Govt. of India.

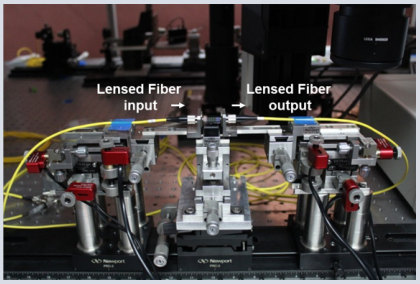


Landmark 2012: When the whole world was progressing fast in the area of silicon photonics technology by taking advantage of their advanced nano fabrication facilities, our PhD research scholar Sujith Chandran was trying desperately to demonstrate photonic wire waveguide using age-old microelectronics fabrication facilities at IIT Madras. However, his efforts finally led to the filing of a US patent, which was granted at a later date.

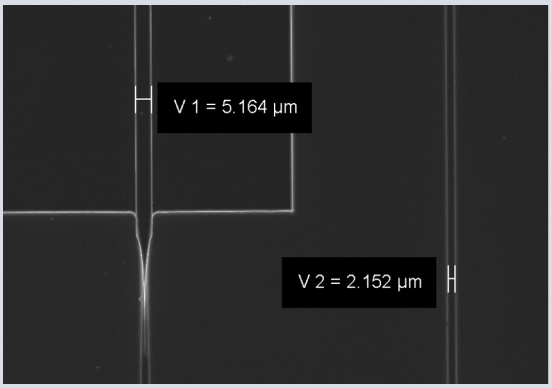


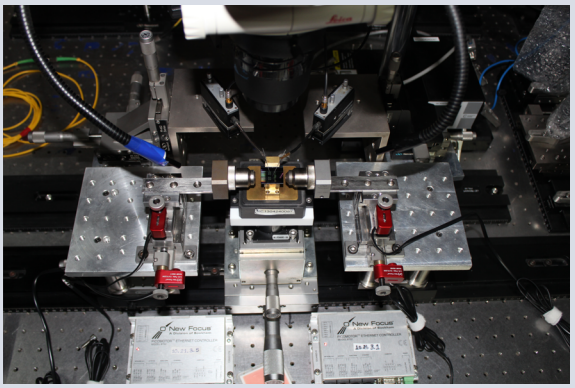




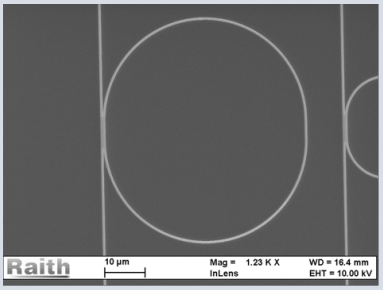


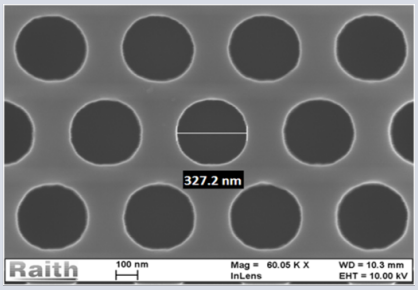
Landmark 2012: Finally, the Centre for NEMS and Nanophotonics (CNNP) was funded by the Department of Electronics and Information technology (DeitY), Govt. of India and our silicon photonics technology started evolving very fast by the hard works of a dedicated team of research scholars led by Sujith Chandran and P. Sakthivel.



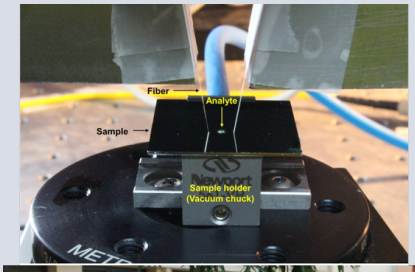


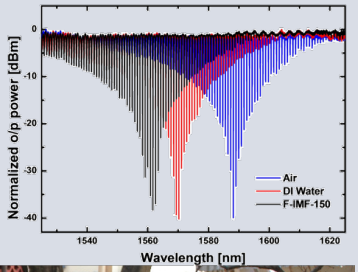
Landmark 2015: The first photonic wire waveguide based microring resonators (MRRs) and photonics crystal structures were demonstrated in silicon-on-insulator (SOI) with device layer thickness of 220 nm (CMOS photonics foundry compatible) using CNNP facilities.





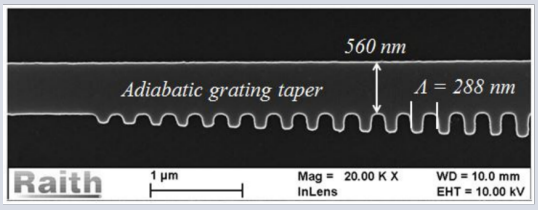
Landmark 2017: A specially designed microring resonator was fabricated to demonstrate evanescent field induced refractive indexing sensing purpose. This was the first silicon photonic wire waveguide device used for lab-on chip sensing application using fiber-optic grating coupling setup in our Integrated Optoelectronics Lab (now moved into CSD108).



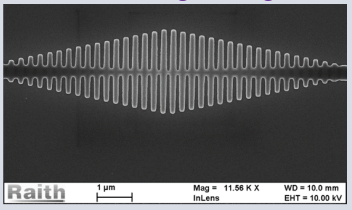


Landmark 2019: Almost all the CMOS fabrication process compatible silicon photonic basic building blocks were demonstrated using in-house fabrication facilities; some of them are with novel design architectures and can be directly used for programmable photonic integrated circuits.

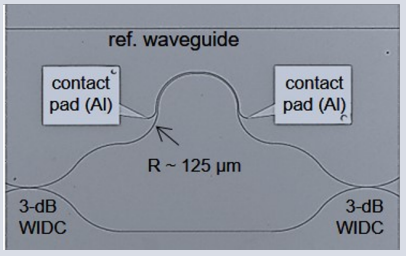
Distributed Bragg Gratings



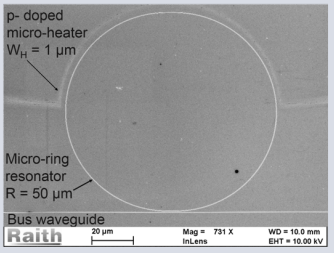
Sub-Wavelength Gratings



Mach-Zehnder Interferometer with Metal Heater



Microring Resonator with Doped Heater



Landmark 2020: The Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits Systems (Silicon Photonics CoE-CPPICS) was proposed with an ambitious list of objectives. It was granted on 29th December 2020 and in midst of Covid'19 Pandemic, the team CoE-CPPICS started working on programmable silicon photonic processors following product research and manufacturing model.

Centre at a Glance

The Centre for Programmable Photonic Integrated Circuits and Systems (CPPICS) is one of the centre of excellence (CoE) initiatives by the Ministry of Electronics and Information Technology (MeitY), Govt. of India. It is hosted by the Department of Electrical Engineering, IIT Madras with a long-term mission for catering R&D in the area of programmable photonic integrated circuits and systems using CMOS compatible silicon photonics technology for solving various levels of complex problems.

Background and Funding Status

The CoE-CPPICS has been established on 1st January 2021 in the Department of Electrical Engineering, IIT Madras with a substantial seed funding of Rs. 2,665 Lakhs (USD 3.5M) from the MeitY, Govt. of India, (Sanction No. GG-11/15/2020/EMCD, dated 29.12.2020), in-kind contribution of Rs. 325 Lakhs (USD 0.5M) from the izmo Microsystems Bengaluru and subsequent additional funding of Rs 425 Lakhs (USD 0.7M) from IIT Madras. This recognition and funding has been possible because of 17 years (since 2006) of R&D work by the Integrated Optoelectronic Research Group led by Prof. Bijoy Krishna Das in the area of silicon photonics technology.

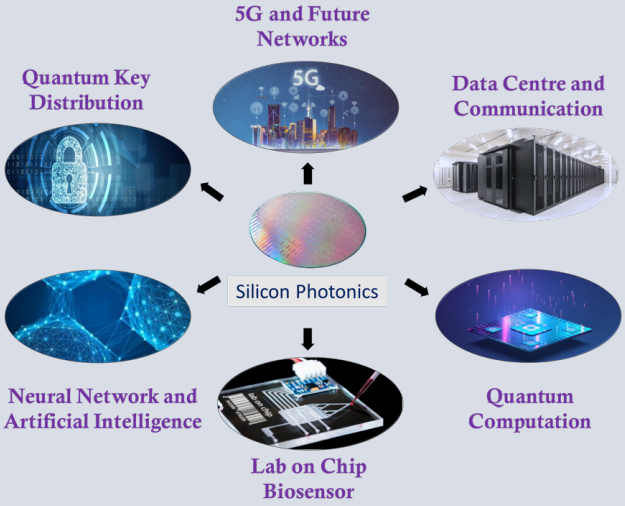
Mission

Our mission is to build capacity in all verticals of silicon photonic integrated circuits manufacturing eco-system through focused R&D and nurture Indian photonics industry for immediate needs in domestic and international markets.

Silicon Photonics CoE-CPPICS Inaugurated on 20th October 2023

The inauguration of our Silicon Photonics Centre of Excellence, graced by the esteemed Shri S Krishnan, Secretary of the Ministry of Electronics and Information Technology (MeitY). This event was further graced by the august presence of Prof. Kamakoti Veezhinathan, Director of IIT Madras and other distinguished individuals, including Smt. Sunita Verma, Scientist G and R&D Group Coordinator (MeitY), Dr. Sankha dip Das, Scientist D (MeitY), Prof. Nagendra Krishnapura (Head of the Department of Electrical Engineering, IIT Madras), Dr. Kishore Kamath, (Vice President of R&D silicon photonics product division, Intel, USA), Dr. Ravi Bhatkal (Managing Director of India Element Solutions Inc, India), Mr. Dinanath Soni (Executive Director of izmo Microsystems, India). Prof. Bijoy Krishna Das, Chief Investigator, Silicon Photonics CoE-CPPICS, IIT Madras, mentioned, "The Silicon Photonics CoE-CPPICS is forging critical partnerships including a strong collaboration with M/s izmo Microsystems in Bengaluru, to deliver state-of-the-art System-in-Package solutions for silicon photonic processor cores. This transformative technology is primed to cater to a wide array of sectors, including quantum computing, quantum communication, 5G/6G communications, IoT, radar, avionics, and more. The nation is looking forward to witnessing the success of CPPICS as it takes this technology to full commercialization and spearheads PIC manufacturing in India. Team CoE-CPPICS has tied-up with SilTerra Malaysia Sdn. Bhd. Silicon Photonics Foundry, Malaysia for wafer scale yield testing of some novel silicon photonic devices already demonstrated using in-house technology at IIT Madras. The team has also signed a MoU with Keysight Technologies USA for joint R&D activities in the area of Silicon Photonics technology".

Current Research Activities



The immediate focus of this CoE is to provide better solutions for microwave and quantum photonics applications such as advanced photonic processors to be used in high-performance RF transceivers, scalable linear optical quantum computing processors for the next-generation qubit computation, and chip-level quantum key generation and distribution circuits, etc. CPPICS is actively developing indigenous PIC design rules and hardware infrastructure for precision packaging for system-level applications.

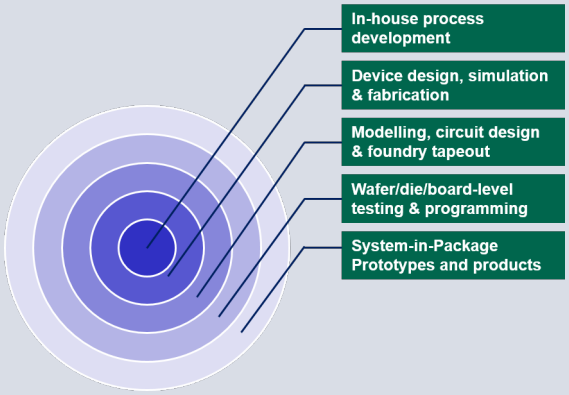
Quantum Information Processing

- Quantum Random Number Generation
- Quantum Key Distribution
- Quantum Sampling Algorithm

Microwave Photonics

- Programmable Radio Frequency Filter
- Optoelectronic Oscillator
- Photonic Beamforming

In our unwavering commitment to driving innovation and fostering technological advancements, we, at the Center of Excellence, are actively engaged in pioneering research starting from technology development to packaging solutions. Our expertise spans a diverse spectrum of domains, with esteemed faculty members from IIT Madras playing an integral role. Their invaluable guidance and expertise are essential to our research endeavors.



Our Experts

Chief Investigator

Prof. Bijoy Krishna Das

The center is being led by Chief Investigator Prof. Bijoy Krishna Das, steering CPPICS toward excellence in research and innovation. Since August 2006, his dedicated efforts have been instrumental in spearheading the development of in-house silicon photonics device technology at IIT Madras.

Chief Technology Officer

Dr. Arnab Goswami

Arnab Goswami joined as the Chief Technology Officer (CTO) of the centre in January 2022. He has been involved in the overall lab infrastructure development, fabrication process development, supervising design and foundry tape-outs. He is also responsible for the creation and execution of self sustenance plan and techno-commercial roadmaping.

Co-Investigators

Prof. Enakshi Bhattacharya
MEMS & Photonics

Prof. Amitava DasGupta
Device Modelling & VLSI

Prof. Nandita DasGupta
Microelectronics & Photonics

Prof. Anil Prabhakar
Quantum Photonics

Prof. Anjan Chakravorty
Compact Modelling

Prof. Deleep R. Nair
Design, Fab and Testing

Prof. Deepa Venkitesh
Fiber Optics & RF Photonics

Prof. Janaki Viraraghavan
Digital IC Design

Prof. Sankaran Aniruddhan
Analog IC design

Prof. Sudharsanan S
Photonics Technology

Prof. Sargunaraj Christopher
Microwave Engineering

Industry Advisory Board

Chairman

As the chairman of CPPICS Industry Advisory Board, I am committed to coordinate with other board members to provide guidance to the team CoE-CPPICS to continue its activities following the Product Research Development and Manufacturing model.

Mallik Tatipamula
CTO at Ericsson
San Jose, California, USA

Members

Albert Pang
CEO
SilTerra, Malaysia

Dinanath Soni
Executive Director
izmo MicroSystems, India

Vivek Raghunathan
Founder & CTO
Xscape Photonics Inc., USA

Arjun Kumar Kantimahanti
R&D Engineer (Optical Systems Division)
Broadcom, USA

Prith Banerjee
CTO, Ansys Inc.
Palo Alto, California, USA

Vikas Gupta
Senior Director
GlobalFoundries USA

Kishore Kamath
Vice President
R&D, Intel Corporation, USA

Kailash Narayanan
President & General Manager
Keysight Technologies, USA

Ravi M. Bhatkal
Managing Director
MacDermid Alpha Electronics Solutions, India

Narayan Srinivasa
Director
Intel Corporation USA

Steve Johnston
Vice President
Merck KGaA Darmstadt, Germany

Vijay Janapaty
Vice President & General Manager
Broadcom Inc., USA

Team Members

Postdoctoral Researchers

Nagarajan Nallusamy
Nonlinear Photonics &
PIC Packaging

Shamsul Hassan
QRNG &
PIC Packaging

PhD Scholars

Suvarna Parvathy
High-Speed Modulator

Ram Mohan Rao Boyapati
Quantum Key Distribution

Ashitosh Velamuri
Microwave Photonics &
Compact Modeling

Anushka Tiwari
SiN Technology Development &
Optoelectronic Oscillator

Pawan Kumar Pandit
High Speed Photodetector &
Feedback Control

Riddhi Goswami
SiN Technology Development &
Photonic Beamforming

Ankan Gayen
QRNG & PIC Packaging

Kumar Piyush
Programmable Photonics &
EIC-PIC Co-Integration

Yash Raj
Programmable Photonics &
Boson Sampling

Anjana James
Compact Modeling &
PDK Development

Dibyanchal Sahu
EIC-PIC Integration

Mayukh Mandal
Integrated Quantum Photonics

Sarad Subhra Bhakat
Si-SiN Hybrid Integration &
SiN technology Development

Shuruti Pandey
Compact Modeling &
PDK Development

MS(Res.)/M.Tech Scholars

Pranita Kumari Swain
SiN Technology Development &
Non-Linear Photonics

Akash Shekhar
EIC-PIC Integration

Manu Maxim
Electronic Oscillator

Rahul Krishna K
Neuromorphic Computing

Chaganti Kamaraja Siddhartha
QRNG

Project Staff

Vinoth S
PIC Packaging

Administrative Secretary

B. Sindhura

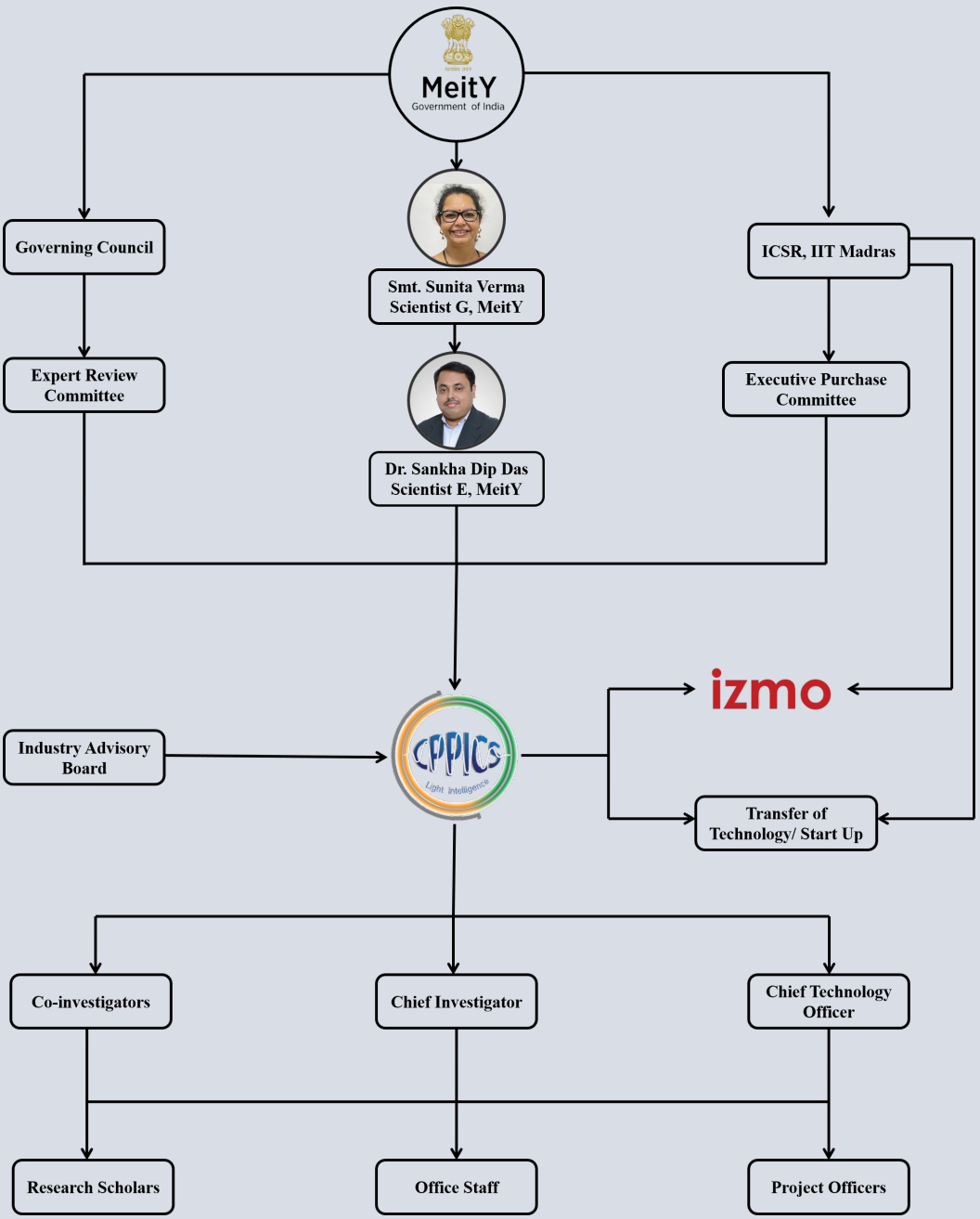
Lab Technicians

Mr. P Saranath

D M Sathish Dev

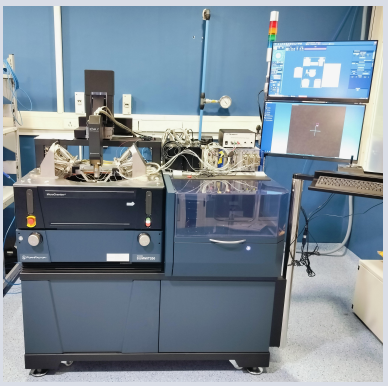
Organizational Structure

This CoE Organization is composed of a Governing Council featuring esteemed members, an Expert Review Committee with exceptional expertise in similar and versatile research areas, Principal and Co-Investigators representing the renowned institution IIT Madras, ICSR – IIT Madras, a Chief Technology Officer, Academic and Industry veterans as collaborators, dedicated and proficient research scholars, dynamic Project Officers, and skilled office staffs.



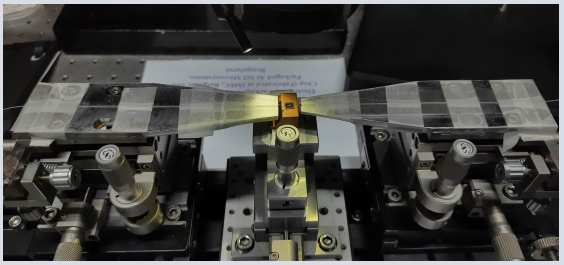
Research Labs and Facilities

In January 2021, our team embarked on an ambitious journey to transform a standard laboratory space into a state-of-the-art design and characterization facility. At CPPICS, we are committed to pushing the boundaries of light-based technologies. Our advanced research facilities and cutting-edge design tools empower researchers and scholars to unlock the immense potential of photonic integrated circuits.



Fully automatic silicon photonics probe station

CPPICS characterization lab



Edge coupling set up

Research scholars during experiments

Research scholars in fabrication process lab

In addition to CPPICS's own facilities, we have in-house fabrication facilities at Center for NEMS and Nanophotonics (CNNP), IIT Madras. The cleanroom within CNNP spans over 2500 square feet and is equipped with state-of-the-art systems for deposition, lithography, etching, and characterization. This robust infrastructure enables us to conduct cutting-edge research and development while maintaining high standards of precision and quality.

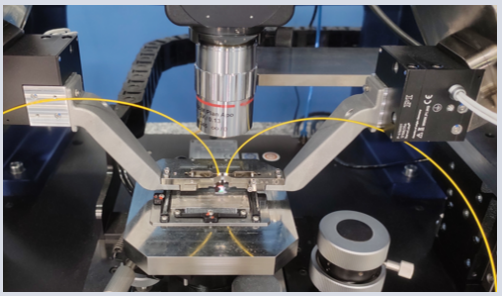
- Electron-Beam Lithography
- DUV and i-line Lithography Systems
- Laser Mask Writer
- LPCVD and PECVD Systems
- Chemical Mechanical Polishing
- Oxidation and Diffusion Furnaces

Major Process facilities

Major Characterization Equipment

- 8 channel superconducting Nanowire Single-Photon Detector System
- Lightwave Component Analyzer and Vector Network Analyzer (26.5GHz & 50 GHz)
- High-Resolution Optical Spectrum Analyzer(Resolution Bandwidth 0.04 pm)
- Real-time Digital Oscilloscope (50 GHz)
- Arbitrary Waveform Generator (50 GHz)
- Wafer-scale silicon photonics probe station

Cleanroom facilities at CNNP



Wafer-scale silicon photonic probe station

State-of-the-Art R&D Activities

At CoE-CPPICS, we drive innovation in photonic integrated circuits through comprehensive R&D, spanning simulation, device design, prototyping, and testing. Our expertise includes compact modeling, waveguide technology on SOI, SiN, and hybrid platforms, as well as device and circuit design. We excel in optimizing programmable photonic circuits for microwave photonics, quantum photonics, and computational applications. In addition, we focus on seamless photonic system integration, emphasizing electronic-photonic cointegration, fiber-optic attachment, and advanced packaging.

Device Design and Compact Modeling

To successfully scale photonic circuits, it is important to analyze the behavior of each device. Creating compact models for basic building devices is crucial. This process empowers photonic designers to develop process design kits (PDKs) and simulate circuits and systems for different applications.

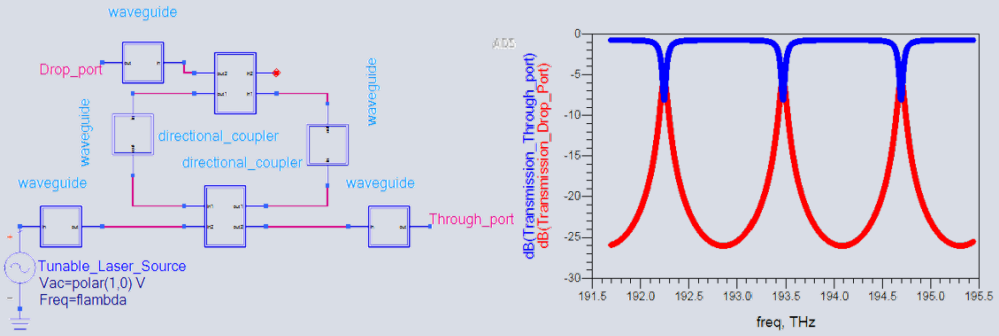
Compact Modelling of Silicon Photonic Devices

Associated Research Scholars: *Shruti Pandey, Anjana James, Ashitosh Velamuri, Suvarna Parvathy, Pawan Kumar, Nagarajan Nallusamy, Shamsul Hassan*

Our group is actively involved in the compact model development of various active and passive photonic components on a chip as well as wafer-scale process variability extraction.

Device modeling: Passive Devices

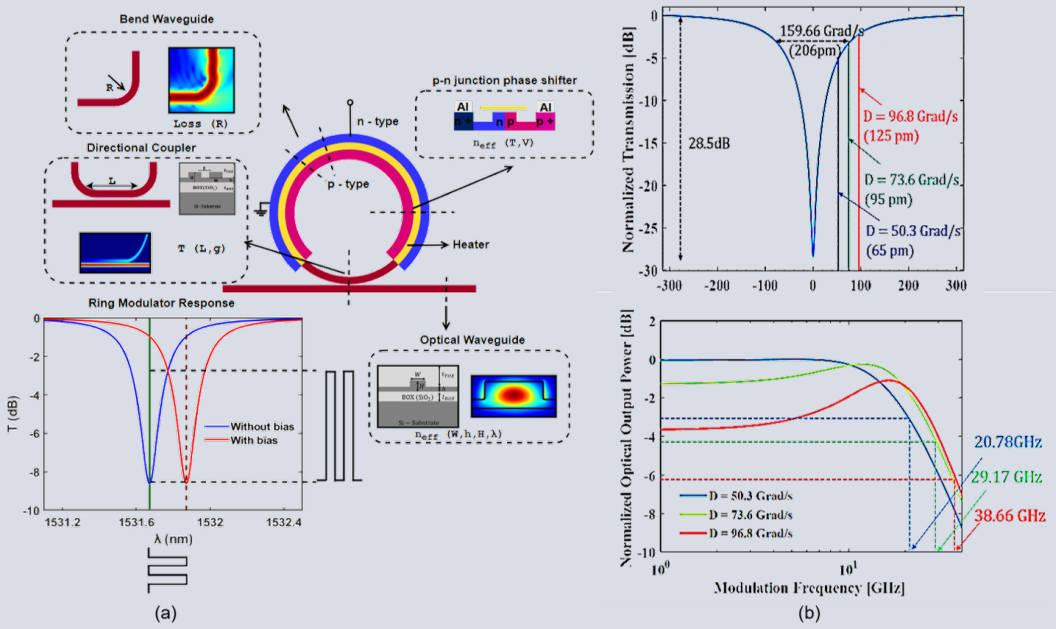
Passive devices like waveguides, directional couplers, ring resonators in all-pass and add-drop configurations, and Mach-Zehnder interferometers are modeled for Spice simulation in EDA tools, which makes it much more time efficient and user-friendly.



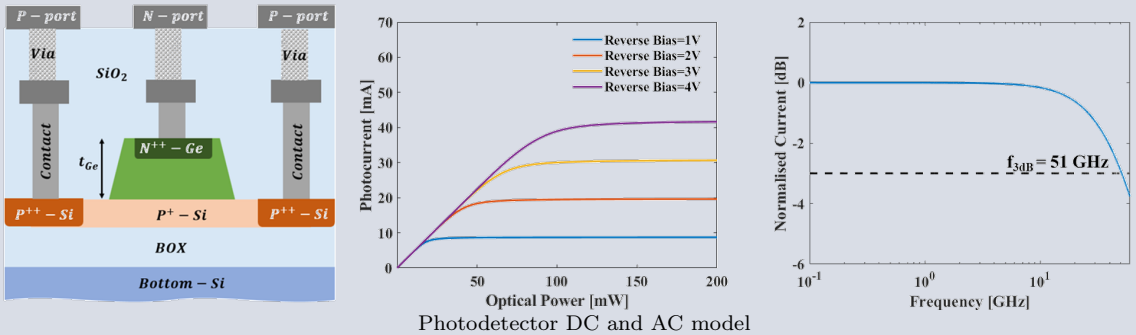
Add-drop ring resonator simulated in ADS

Device modeling: Active Devices

The modulator and photodetector are important components for the realization of an RF photonic link. An accurate model linking the device performance to the design parameters of the device will help the designers to design without going through time-consuming photonic and charge simulations. After running a lot of optical and electrical simulations, we have implemented a preliminary model to give us the linear and non-linear response of the modulator and photodetector. The AC and DC responses of both devices are simulated using our model, and the results are given in the figures below.



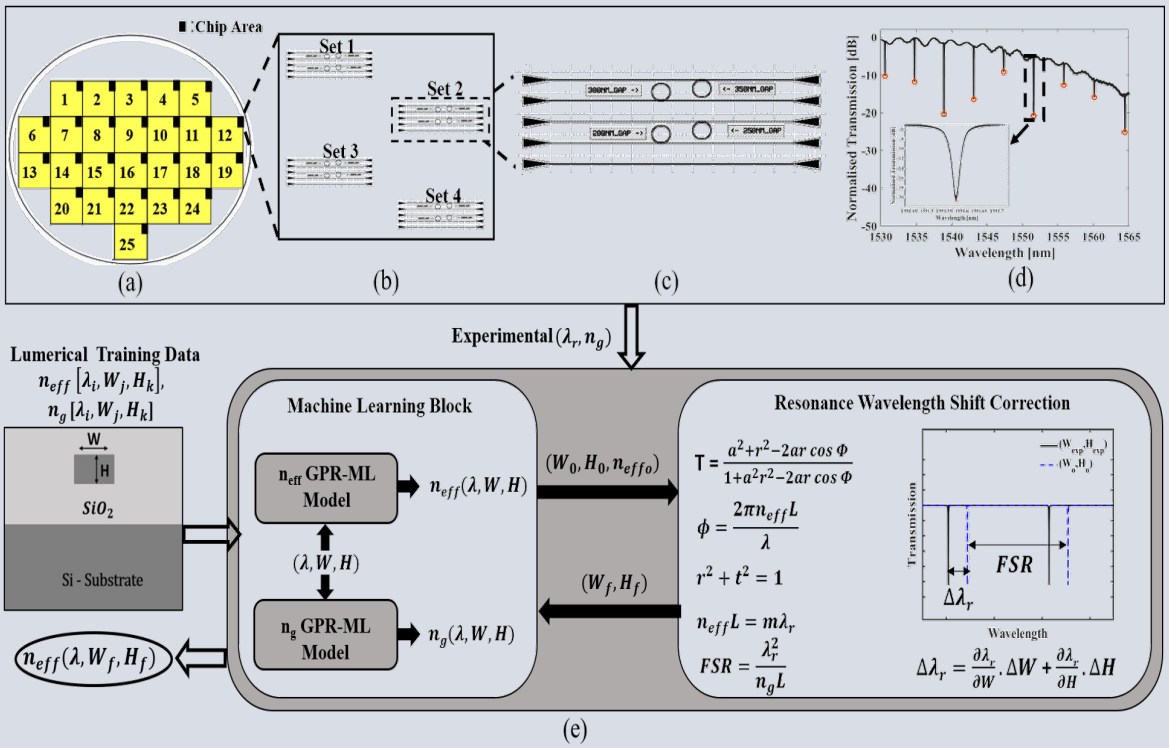
Microring modulator compact model: Individual components are separately modeled and combined for the microring modulator system-level model



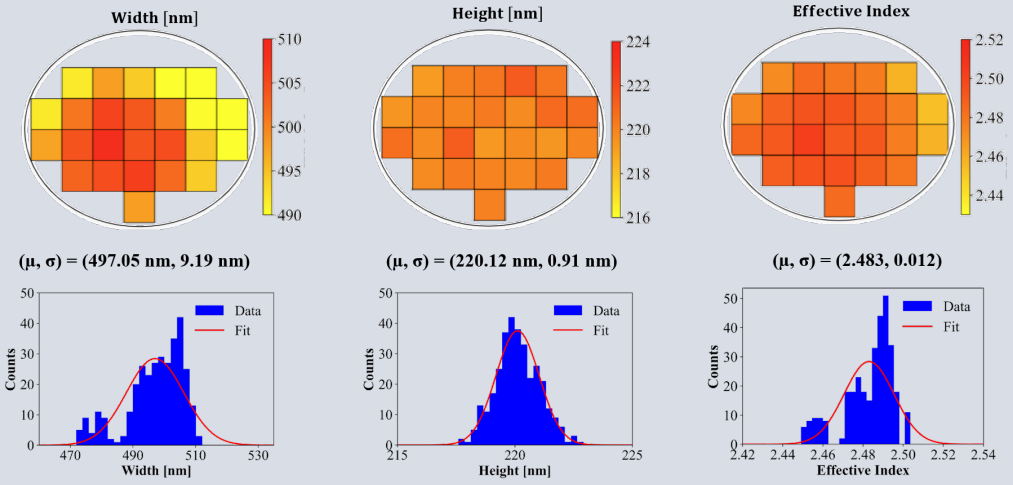
Photodetector DC and AC model

Wafer-scale process variability extraction

A Machine Learning (ML)-enhanced algorithm has been developed for the prediction of fabrication process-induced wafer-scale (200-mm) variability, which is computationally faster and has high accuracy in predictions. The algorithm proposed for the prediction of waveguide dimensional variability (and effective index of guided mode) uses data from the experimental characterizations of the racetrack microring resonator (MRR) in an all-pass configuration fabricated across a 200mm silicon-on-insulator (SOI) using the SilTerra silicon photonics fabrication process line. The algorithm is described in the figure above. Wafer-scale width, height, and effective are obtained using the proposed algorithm.



ML enhanced algorithm for wafer scale process variability extraction: (a)Reticle numbering and relative location of devices; (b)Layout; (c) zoomed layout; (d) typical spectral response of the MRRs; and (e) flowchart representing the proposed algorithm with the relevant equations used.



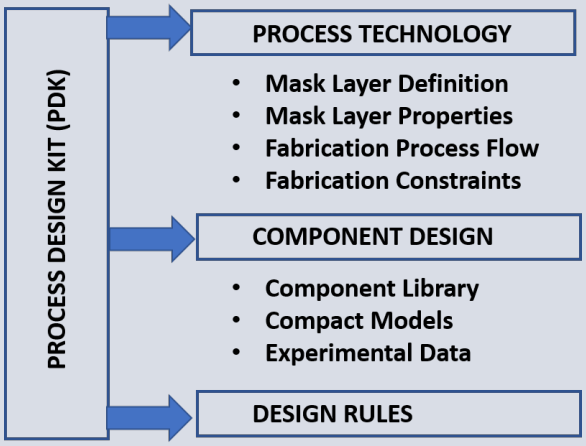
Wafer-map representing width, height, and effective index variation and distribution across wafer.

We also look forward to realizing electronic photonic co-simulation using electronic design automation tools to simulate large-scale electro-optic circuits for applications like LIDAR, neuro-morphic computing, and quantum computing.

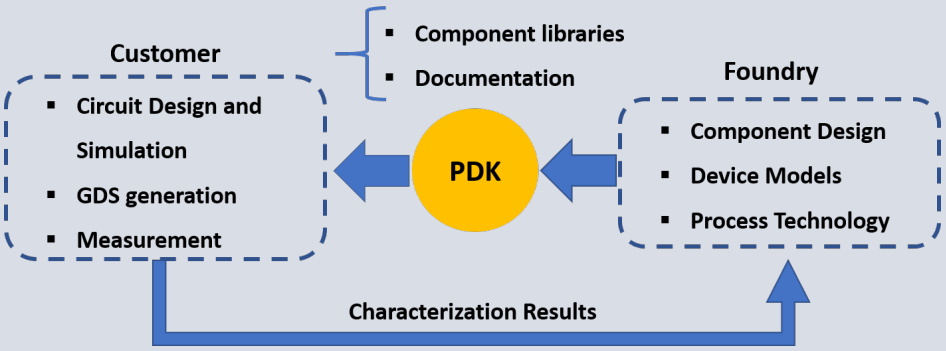
Process Design Kit Development

Associated Research Scholars: *Arnab Goswami, Pawan Kumar, Ashitosh Velamuri, Kumar Piyush, Ram Mohan, Suvarna Parvathy*

A Process Design Kit (PDK) bridges circuit designers and foundries, enabling efficient photonic circuit design and fabrication. It includes process details, fabrication constraints, and a library of analytical or physics-based models for passive (e.g., waveguides, splitters, grating couplers) and active (e.g., modulators, photodetectors) components. Designers use these libraries to create GDS layouts for fabrication and, in large-scale designs, simulate circuit performance using PDK-compatible blocks before fabrication. The PDK also incorporates experimental data, design rule checks, and is continually updated based on characterization results of fabricated devices to ensure accuracy and compatibility.

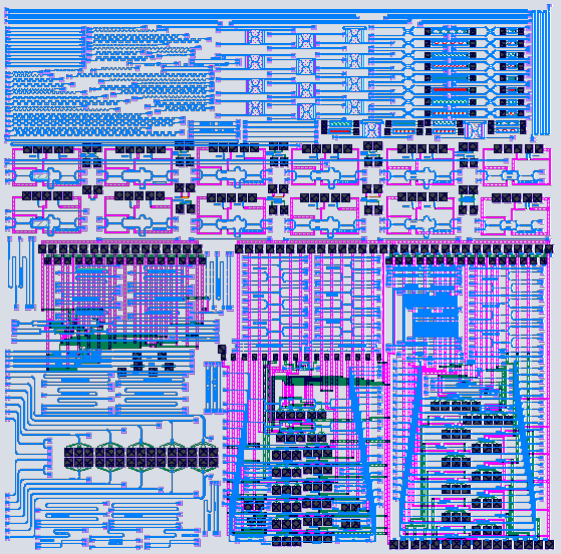


PDK serves as a link between the circuit designer and the foundry enabling the circuit designer to design photonic circuits using the different components available in the component library. The component library is in the form of analytical or physics-based models for the basic passive (waveguides, waveguide bends, power splitters, grating couplers) and active (modulator, photodetector) photonic devices. Based on these available component libraries, the customer designs the GDS layout and submits the design to the foundry for fabrication. For large-scale photonic circuit design, there can be PDKs that offer photonic circuit simulator-compatible blocks, which will enable the designer to evaluate the circuit performance well before the actual fabrication. The layout of the desired circuit is shared with the foundry, following which mask preparation and fabrication are carried out. Based on the characterization results of the fabricated devices, required updates are made to the existing PDK.

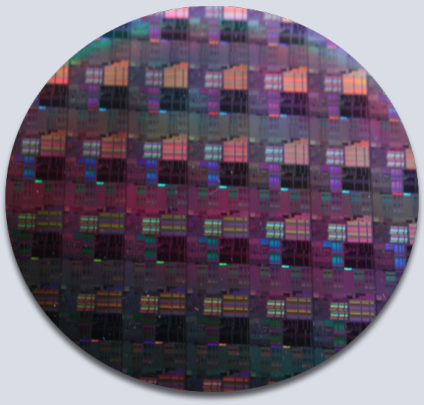


SilTerra joins hands with CPPICS

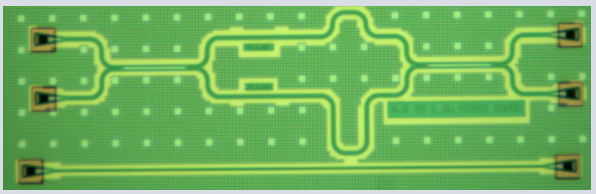
One of the leading global semiconductor foundries, SilTerra, Malaysia has joined hands with CPPICS to develop silicon photonics PDK. For our first run of tape out, our scholars have designed different passive components which includes waveguides, waveguide bends, power splitters, wavelength filters and Mach Zehnder Interferometers. The structures given for tape out have been fabricated by SilTerra, and the optical characterization of the fabricated devices is actively being carried out at CPPICS. These characterization results will be modeled to form our first-cut PDK for SilTerra. This run will be followed by active device fabrication, characterization, and modeling. We are also looking forward to developing models for devices like distributed Bragg reflectors (DBR), waveguide crossings and microring based filters which are not available currently in any other existing foundry PDK.



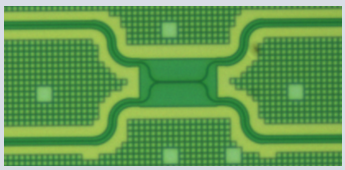
Layout design of various active and passive devices on 8 mm × 8 mm chip, for tape-out from SilTerra



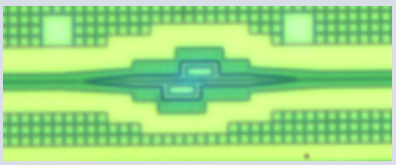
8 inch wafer fabricated at SilTerra, Malaysia



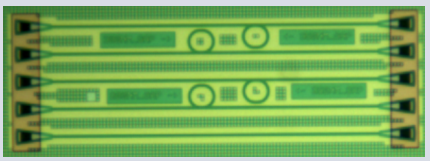
Microscopic image of fabricated unbalanced MZI with reference waveguide



Microscopic image of fabricated directional coupler

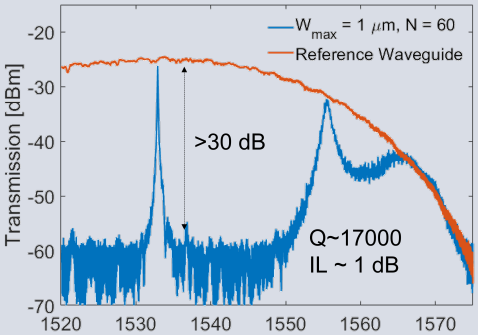


Microscopic image of fabricated distributed Bragg reflector

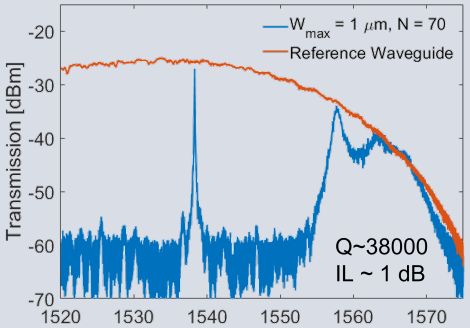


Microscopic image of fabricated microring resonator with grating couplers

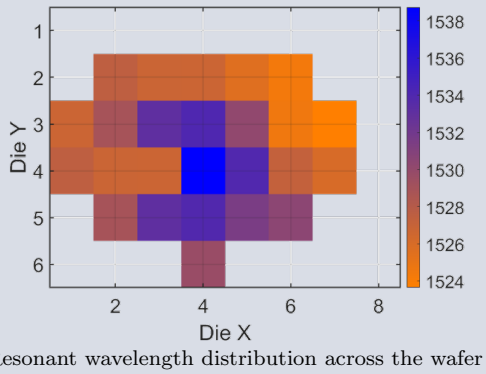
We demonstrated a compact singly resonant DBR cavity with broadband DBR mirrors using SilTerra's 200 mm silicon photonics foundry process line. The wafer-scale yield has been analyzed in terms of resonance wavelength and quality factor.



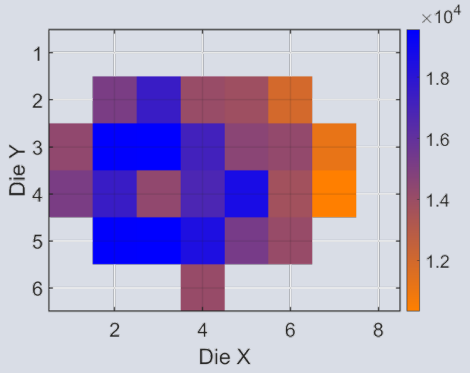
Typical device characteristics



Typical device characteristics



Resonant wavelength distribution across the wafer



Quality factor distribution across the wafer

The standard deviation of the resonant wavelength and quality factor is found to be 3.735 nm and 2650 respectively. The fabrication yield comes to reasonably good but there is a scope for improvement by fine tuning the design and process parameters. Nevertheless, these results are promising for the future inclusion of a DBR-based Fabry-Pérot resonator in the device libraries of commercial silicon photonics PDK, as various active and passive components for large-scale integration.

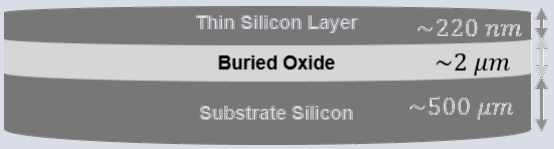
Fabrication Process Development

We at CoE-CPPICS are working in two different technology platforms i.e. Silicon on Insulator (SOI) and Silicon Nitride on Insulator (SNOI). Over the past 15 years, we have achieved a high level of maturity in SOI waveguide technology processes. This advancement has allowed us to demonstrate various innovative passive devices, circuits, and phase shifters for multiple applications, maintaining a waveguide loss of less than 5 dB/cm. For the past 2 years, we have been involved in developing in-house SNOI waveguide technology process starting from bare silicon wafer, growing silicon di-oxide on it, followed by LPCVD silicon nitride deposition. Very recently, we have achieved the low loss waveguide with propagation loss below 1 dB/cm. To further reduce the loss we are working constantly to refine our fabrication process steps and have also started working on damascene process. Furthermore, we are also actively working towards the hybrid integration of Si and SiN to demonstrate efficient circuits in terms of lower loss and thermal budget.

SOI Waveguide Technology

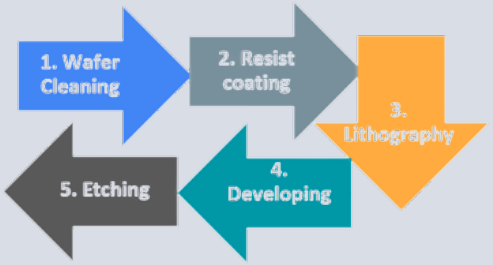
Associated Research Scholars: *Suvarna Parvathy, Ram Mohan, Arnab Goswami, Ashitosh Velamuri, Ankan Gayen, Kumar Piyush, Pawan Kumar, Yash Raj*

SOI wafers consist of a thin layer of silicon (the device layer), buried oxide and silicon substrate stacked one above another as shown below. The thin silicon layer is used to fabricate waveguides and other passive or active optical devices. The buried oxide prevents propagation of light into the silicon substrate thereby supporting optical modes in tne device layer guided by total internal reflection.



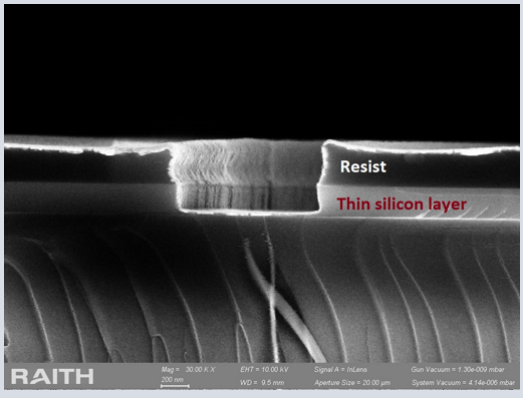
SOI wafer

Fabrication flow of optical devices on SOI includes several process steps. We have shown the major steps here. First, we start with cleaning of SOI wafer which includes standard organic cleaning to remove oils followed by inorganic cleaning to remove metallic oxides. After cleaning we need to dehydrate the wafer to remove any water content. Now, we can go for resist(positive/negative) coating. Afterwards on this coated sample, pattern is transferred from mask either using E-beam lithography or photo-lithography.



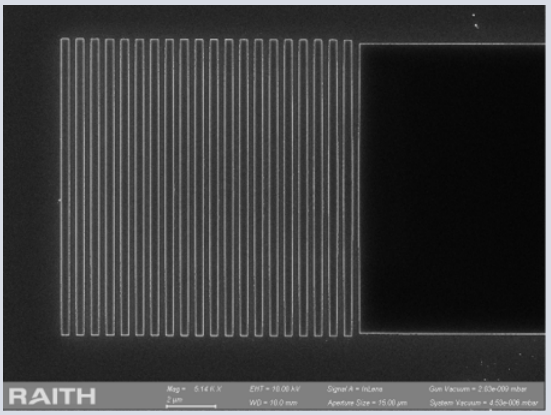
SOI process flow

Once, the pattern is transferred, this wafer is put into developer solution to remove the exposed/unexposed resist (depending on resist type). After developing we go for etching to get our final devices (passive).

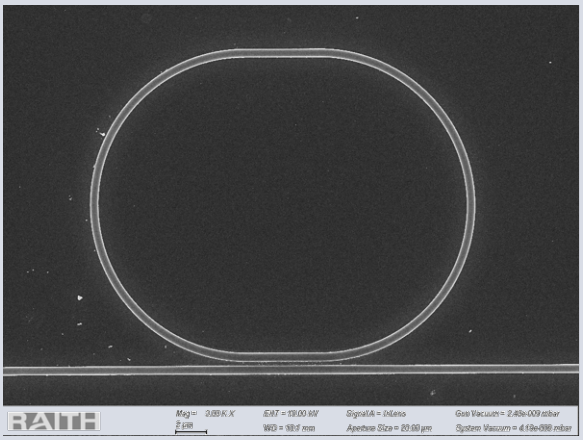


SEM cross-section view of etched device on SOI

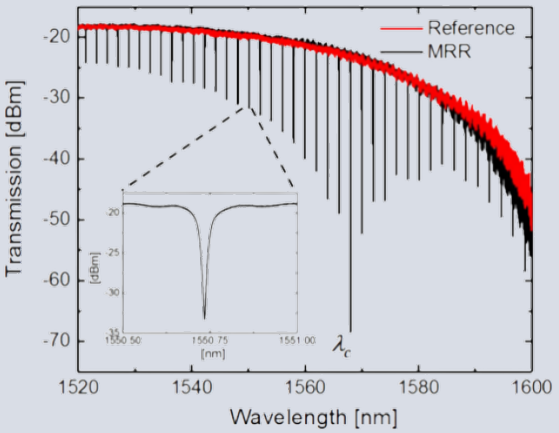
The core research of our group involves novel device designs, CMOS compatible fabrication process optimizations and subsequent experimental demonstrations leading towards cost-effective, energy-efficient and high-speed silicon photonic circuits for various applications. As of now, various prototype and packaged devices like power splitters, channel interleavers, variable optical attenuators, p-i-n phase shifters/modulators, ring resonators, DBR (Distributed Bragg Reflector) and SWG (Sub-Wavelength Grating) filters etc., have been demonstrated by utilizing the resources at our centre of excellence CPPICS and nanofabrication facilities at IIT Madras.



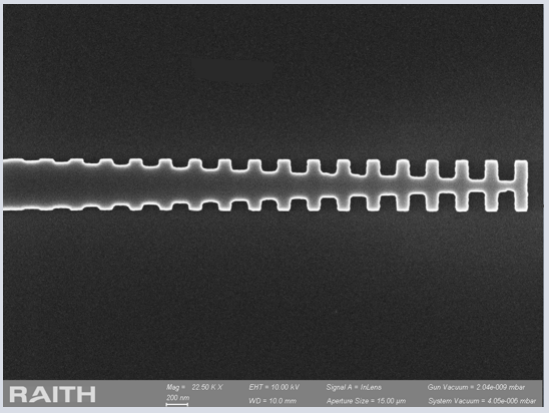
SEM top view of grating coupler on SOI



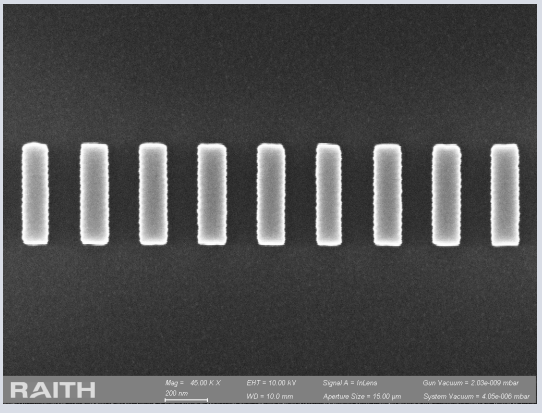
SEM top view of a Micro Ring Resonator on SOI



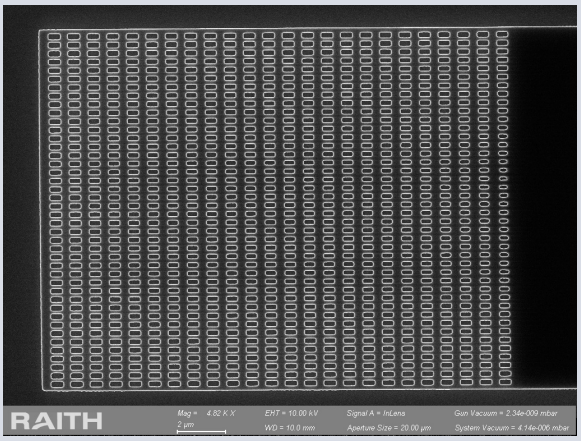
Measured transmission characteristics of a Micro Ring Resonator along with a reference waveguide



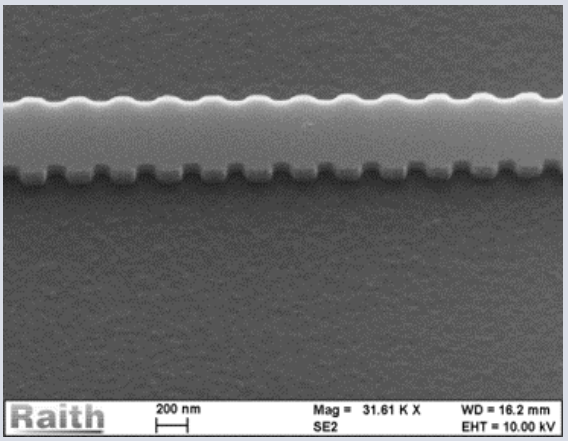
SEM top view of SWG Taper on SOI



SEM top view of SWG waveguide on SOI

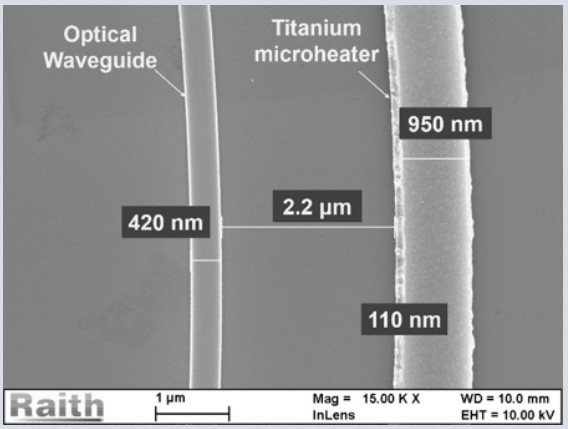


SEM top view of 2-D grating on SOI

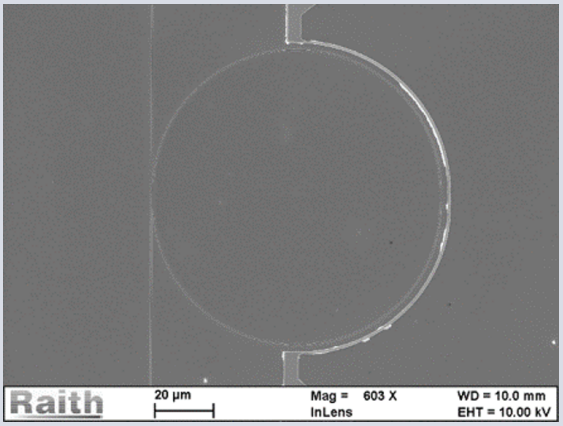


SEM angled view of DBR on SOI

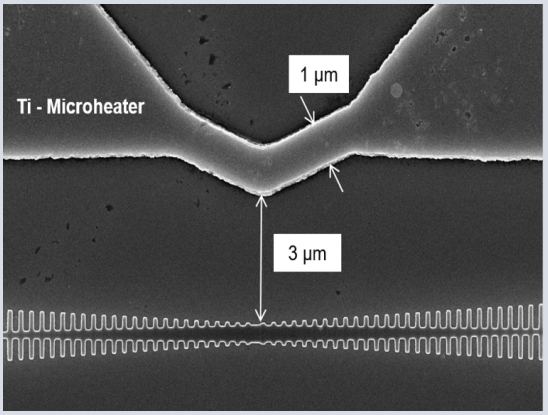
To address the fabrication imperfections and to operate these devices at specific working points or to switch between different states, active control is essential. One way is to use thermo-optic modulation by placing micro-heaters either at the side or on top of the waveguides and using heating to change the refractive index. Fabrication of these heaters starts once the passive devices are patterned. Since positioning of the heaters demand high precision, we use E-beam lithography. Aluminium (Al) is used for contact padS and Titanium (Ti) for metal heater fabrication. Below we have shown a MicroRing Resonator (MRR) of $50\mu m$ ring radius with side Titanium (Ti) side heater.



SEM zoomed-in view of MRR with side heater



SEM top view of MRR with side heater

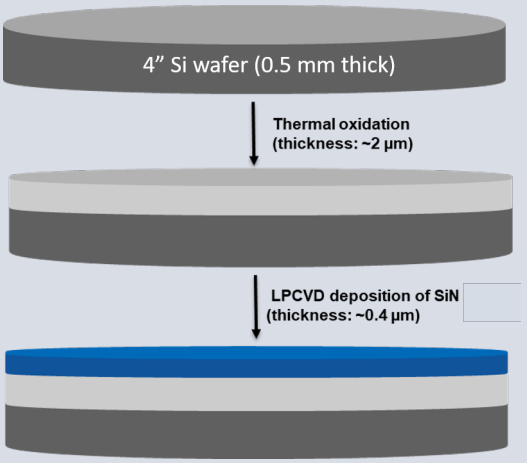


SEM zoomed view of DBR cavity with side heater

SiN Waveguide Technology

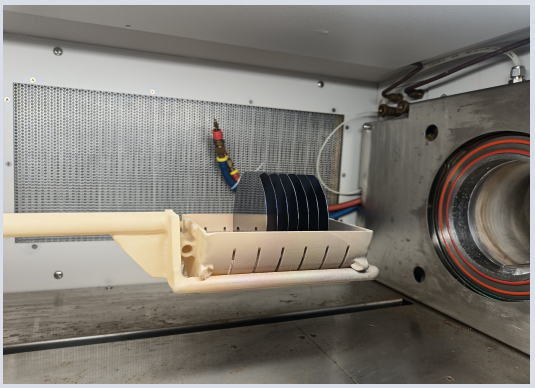
Associated Research Scholars: *Riddhi Goswami, Pranita Ku. Swain, Anushka Tiwari, Sarad S. Bhakat*

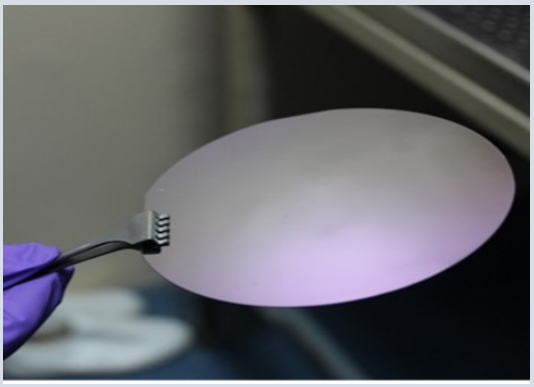
In addition to Si core, SiN (Silicon Nitride) is gaining major attention due to its relatively lower waveguide losses, wider transparency and less sensitivity to temperature fluctuations and fabrication variations. The growth of an optical grade oxide layer (for bottom cladding) and subsequent deposition of SiN device layer are the most important aspects for the realization of large-scale photonic integrated circuits with acceptable waveguide losses and fabrication yields. Our group has been working towards fulfilling that goal and has made conceivable achievements so far.We are able to grow good quality thermal oxide wafers($\approx 2\mu m$) and stoichiometric, crack-free SiN wafers($\approx 0.4\mu m$) with excellent wafer scale variations.



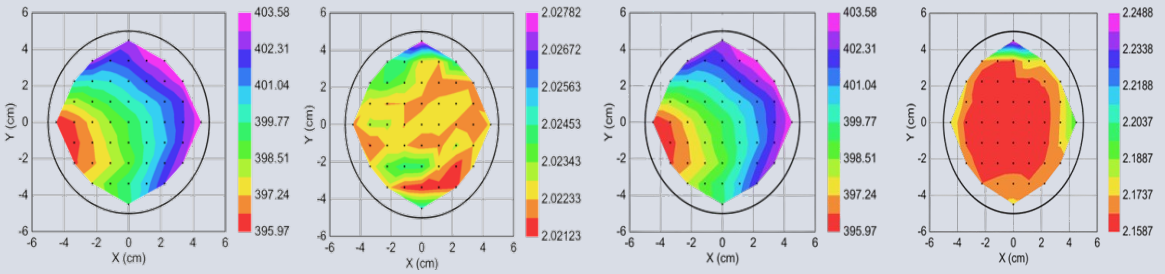
SiN Deposition Process Flow

We have also been able to demonstrate losses below 1 dB/cm and 3 dB/cm in LPCVD (Low Pressure Chemical Vapour Deposition) and PECVD (Plasma Enhanced Chemical Vapour Deposition) SiN platforms (both on $2\mu m$ thermal oxide) respectively using traditional waveguide technology like the SOI process which involves patterning on device layer. Both the platforms were developed completely indigenously here at IITM starting with 4 inch bare Si wafer.


Loading of thermal oxide wafers in SiN furnace


In-house fabricated SiN wafer

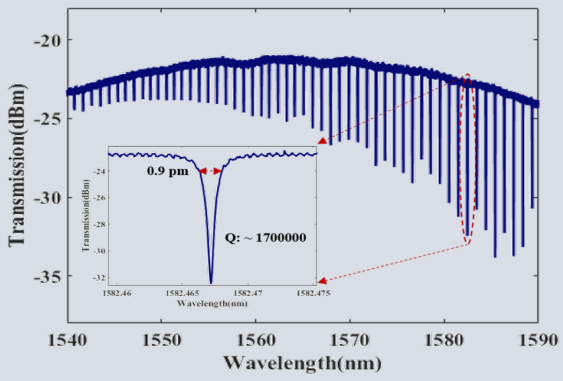
Although LPCVD SiN provides low-loss waveguides, the thickness is limited to 400 nm due to tensile stress within the film. However in order to harness the nonlinear properties of SiN, we need relatively thicker films for demonstrating applications such as frequency comb generation. We have



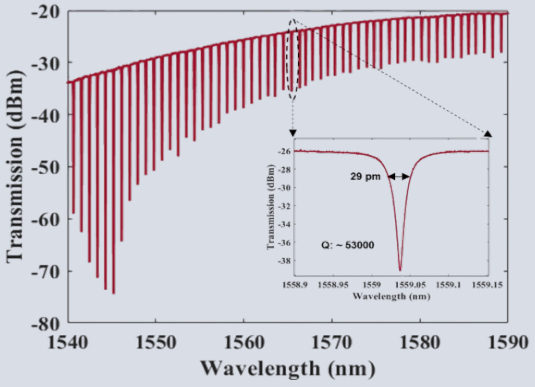
LPCVD SiN PECVD SiN

Wafer scale ellipsometric measurements showing thickness and refractive index variations (at 1550 nm) respectively

also, already established a process flow for Damascene which can provide efficient stress control and prevent cracks in the film (for higher thickness of SiN, >400 nm). The process is based on first etching trenches into buried oxide (BOX) layer and then filling the trenches with SiN for waveguide core and finally planarizing the surface with Chemical Mechanical Polishing (CMP). A top oxide layer may be deposited later depending on requirements. Damascene is expected to give lesser waveguide losses since we are not directly etching the SiN device layer leading to improved side-wall roughness. Low loss, planar optical waveguides have the potential to be a key enabling technology for a wide range of applications, such as delay lines, ultra narrow linewidth lasers, nonlinear photonic devices such as soliton Kerr frequency combs or quantum photonic circuits. Below attached are the MRR (Micro Ring Resonator) responses on the two different SiN platforms (fabricated with standard waveguide technology that involves etching of device layer).



MRR response on LPCVD SiN

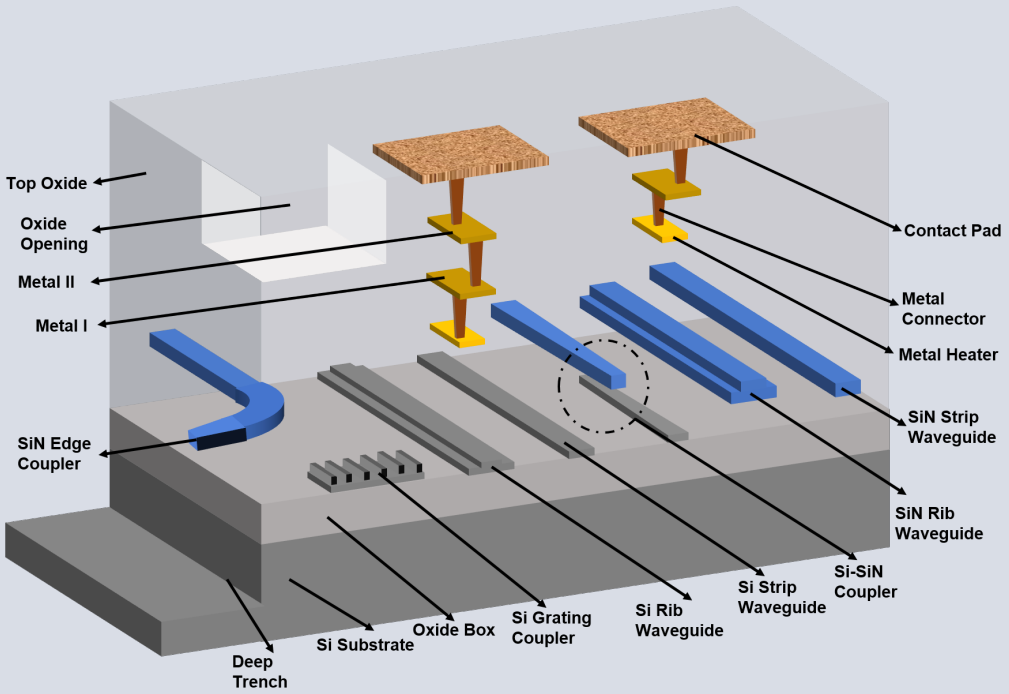


MRR response on PECVD SiN

Si/SiN Hybrid Waveguide Technology: In-House Process Development

Associated Research Scholars: *Sarad S. Bhakat, Riddhi Goswami, Anushka Tiwari, Pranita Ku. Swain.*

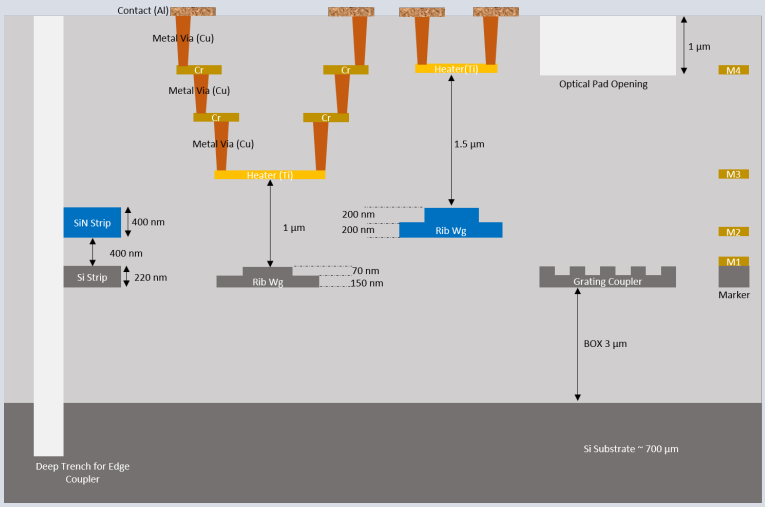
The rapid development of fabrication techniques has boosted the resurgence of silicon-based Photonic Integrated Circuits (PICs). The silicon-on-insulator (SOI) and Silicon Nitride (SiN) platforms have been extremely successful in PIC development due to their CMOS compatibility. The devices are usually fabricated on a wafer following a planar process, where only one core material with a defined thickness is included. This traditional single-material platform cannot provide all the functionalities required for fully integrated PICs. By embedding thin-film SiN onto the SOI platform, Si/SiN hybrid photonic devices can be integrated on the same chip, simultaneously leveraging the advantages of both material platforms.



3D schematic representation of a hybrid Si/SiN photonic integrated circuit (PIC) Platform

Currently in PIC material technologies, no waveguide material can address the needs of all the potential applications of PICs. Therefore advanced PICs may require the best possible performance of a large number of different photonic elements in PICs to achieve the desired functionalities, which may not be possible with single waveguide material technology. The above figure showcases a 3D schematic of a hybrid Si/SiN photonic integrated circuit (PIC) designed for advanced optical and photonic applications. Key components include SiN strip and rib waveguides, Si strip and rib waveguides, and Si-SiN couplers that enable efficient light transmission and coupling between waveguide layers. The deep trench enhances isolation, while grating couplers and edge couplers facilitate light input/output.

The metal heater assembly, with connectors and contact pads, ensures precise thermal control critical for tuning optical properties. Oxide layers provide electrical insulation and mechanical stability. This hybrid design combines silicon's compactness with silicon nitride's low-loss characteristics, making it ideal for high-performance photonic systems.



Cross-sectional view of a hybrid Si/SiN photonic integrated circuit (PIC)

This cross-sectional schematic highlights the intricate structure of a hybrid silicon-nitride photonic integrated circuit (PIC), emphasizing its multi-material integration. The diagram showcases SiN strip waveguides designed for low-loss optical routing, Si rib and strip waveguides for compact light confinement, and grating couplers for seamless light coupling. A deep trench ensures effective edge coupling, while the titanium metal heater, supported by chromium and copper vias, enables precise thermal tuning. The buried oxide (BOX) layer and silicon substrate provide the foundation for thermal insulation, mechanical support, and optical stability, enabling the hybrid PIC's high performance.

Hybrid Si/SiN integrated photonic devices offer distinct advantages over single-platform devices in two key applications. First, high-speed modulators and photodetector arrays can be fabricated on the well-established Silicon-on-Insulator (SOI) platform, widely recognized for its efficiency in active modulation. Second, for passive components like routing waveguides and delay lines, the low-loss characteristics of SiN material significantly enhance performance. These hybrid devices combine the strengths of both materials, minimizing optical losses, reducing power consumption, and enabling advanced high-density integration for PICs.

	Silicon Nitride	Silicon-on-Insulator
Wavelength range	0.3 µm – 3 µm	1.1 µm – 4.5 µm
Lasers, Amplifiers	NA	NA
Photodetectors	NA	++
Modulators	NA	+
Thermo-optic phase shifter	++	+++
Low-loss passive devices	+++	++
Fiber to chip coupling	+++	++
Packaging	+++	+++
Electronic-Photonic Co-integration	+++	+++

+++ : excellent, ++ : very good, + : good

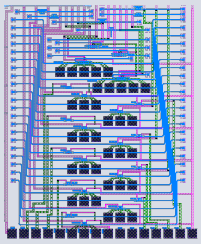
Photonic Circuits and Processors

Photonic circuits have diverse applications, spanning from Programmable Photonics, featuring versatile photonic processors, to Microwave Photonics, incorporating RF filters and optoelectronic oscillators. They also find applications in Quantum Integrated processors, which utilize photon sources, Quantum random number generators, Quantum key distribution, and Quantum processors.

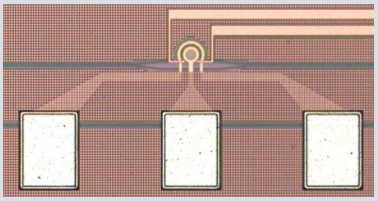
Active devices: Modulators and Photodetectors

Associated Research Scholars: *Suvarna Parvathy, Pawan Kumar*

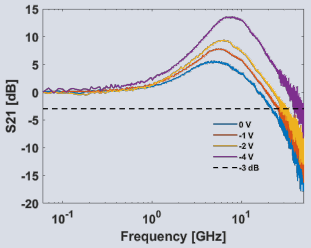
Modulators and photodetectors are major components in any integrated photonic circuit, performing the electrical-optical and optical-electrical conversion of signals respectively. It is essential to have high efficiency and high bandwidth modulators and detectors for efficient and ultra-fast signal processing applications.
Modulation of light in silicon platform can be achieved by plasma or free carrier dispersion. The widely used modulation element is a waveguide with a p-n junction doped on it, which is operated under reverse bias. The application of voltage to the diode changes the free carrier concentration and thus the effective refractive index of the waveguide. This in turn results in a shift in the optical transmission characteristics of the device. The p-n doped waveguide or the p-n phase shifter can be integrated into various photonic devices like Mach-Zehnder Interferometer (MZI), Microring Resonator (MRR), Microdisc Resonator (MDR) to form respective modulators - MZM, MRM, MDM etc. Devices like distributed Bragg reflectors, photonic crystals have also been used for implementing modulator. Some of the important performance metrics of modulators are bandwidth, phase efficiency, extinction ratio, insertion loss, modulation amplitude, and footprint. As compared to interferometric modulators like MZM, resonant-based modulators like MRM, MDM have much lesser footprint and become a preferred choice for wavelength division multiplexing (WDM) applications.



Layout of microring, microdisc modulators fabricated from SilTerra

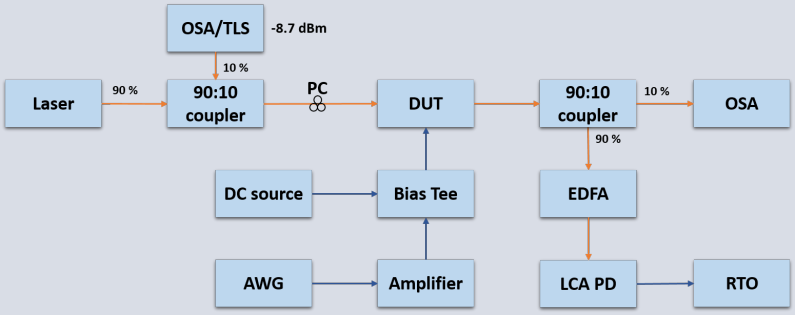


Microscopic image of all-pass ring modulator (10 μm radius) fabricated from IMEC



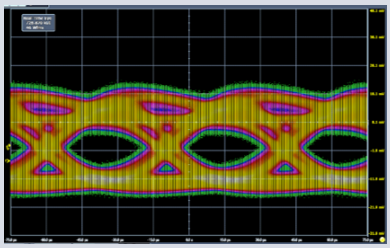
Electro-optic S21 response of MRM for different reverse bias voltages fabricated from SilTerra

We have fabricated compact microring modulators of 5 μm radius, and microdisc modulators of 10 μm radius from IMEC, Belgium as well as SilTerra, Malaysia that can operate up to 50 GHz. The 3 dB cut-off frequency of a microring or microdisc modulator is largely decided by the quality factor of the device, and the RC time constant of the p-n junction. As the reverse bias on the p-n junction increases, the cut-off frequency of the modulator also increases, since the time constant decreases.

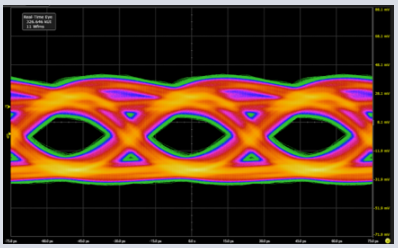


Experimental set-up for OOK modulation. OSA: Optical Spectrum Analyzer, TLS: Tunable Laser Source, DUT: Device Under Test, EDFA: Erbium Doped Fiber Amplifier, AWG: Arbitrary Waveform generator, LCA: Lightwave Component Analyzer, PD: Photodetector, RTO: Real Time Oscilloscope

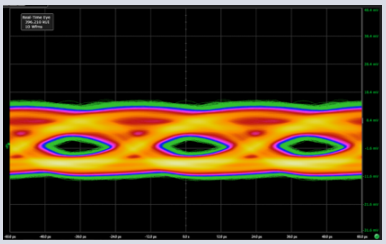
Digital on-off keying (OOK) modulation was studied at 10, 20, 25 Gbps speeds using a PRBS7 pseudo random sequence from an arbitrary waveform generator. It was observed that at higher input optical power, the modulation amplitude of the modulated eye diagram increases. The modulation amplitude degrades as speed of the signal increases as expected due to the low-pass frequency response of the modulator.



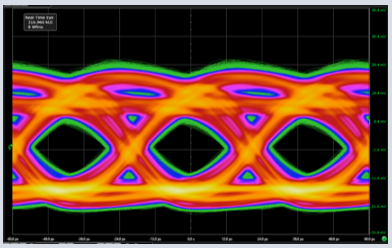
Eye diagram of microring modulator (IMEC) at 20 Gbps at low optical power (y-scale: 10 mV/div)



Eye diagram of microring modulator (IMEC) at 20 Gbps at high optical power (y-scale: 20 mV/div)

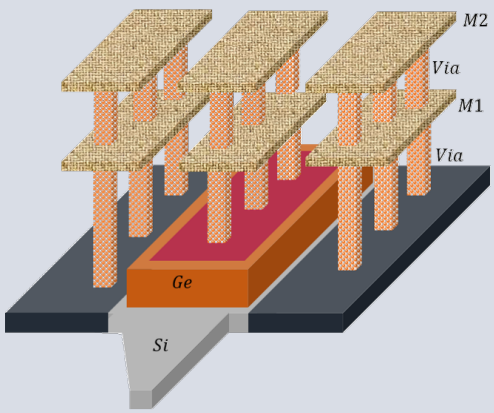


Eye diagram of microring modulator (IMEC) at 25 Gbps at low optical power (y-scale: 10 mV/div)

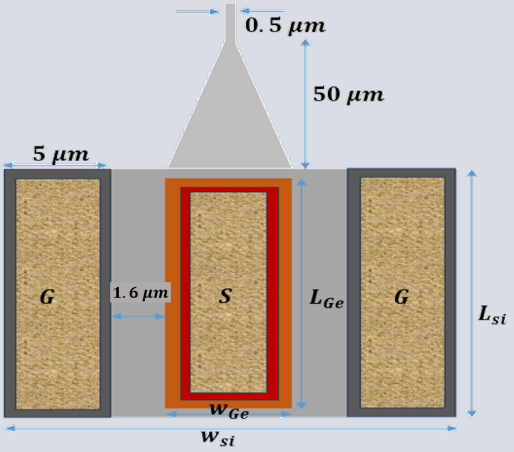


Eye diagram of microring modulator (IMEC) at 25 Gbps at high optical power (y-scale: 10 mV/div)

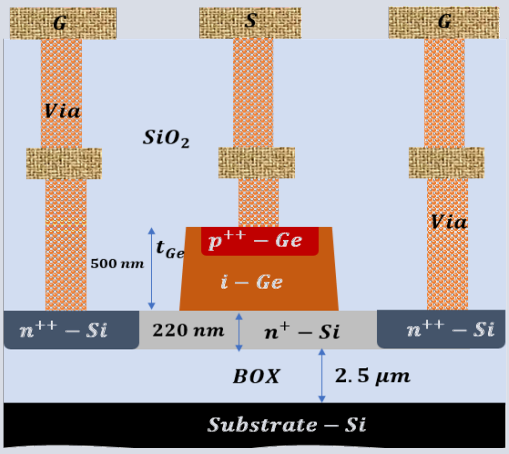
Silicon is transparent in telecommunication band (1310 - 1600 nm). Therefore, On chip detection in silicon photonics platform, we need another materials which can absorb light around above band and are compatible to CMOS fabrication process. Germanium is one, which is extensively used in silicon foundry for on chip detection. Recently, a variety of high-performance Ge photodetectors have been demonstrated on silicon photonic platforms by different research group using different silicon photonics foundries. Advancement of waveguide integrated germanium photodetectors (Ge PDs) holds crucial research significance for both academia and industry. The geometry and wavelength dependent characteristic of Ge photodetector has been comprehensively evaluated by our group in collaboration with Silterra, Malaysia. The measurement result show the low dark current, high responsivity, high bandwidth and high power saturation in single injection configuration. This study serves as a significant reference point to waveguide integrated photodetector in silicon photonics.



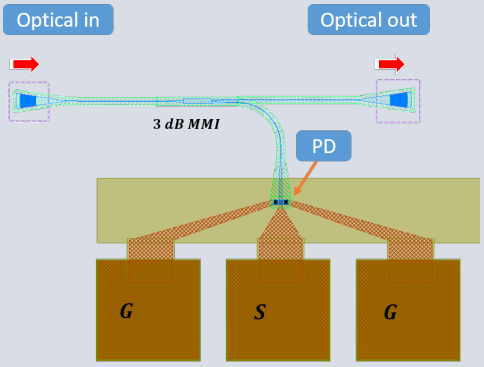
3D view of Ge on Silicon Photodetector



Top view of Ge on Silicon Photodetector

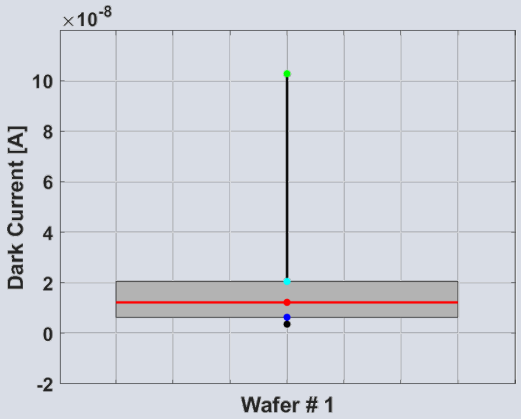


Cross-Section view of Ge on Silicon Photodetector

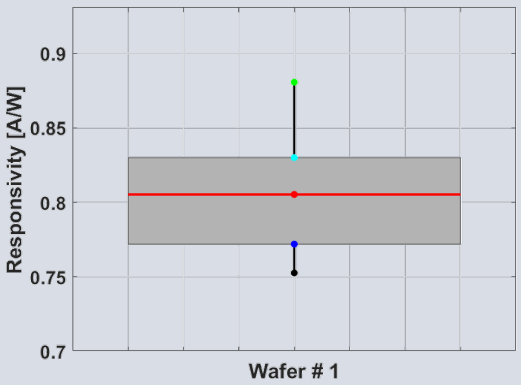


Complete Layout view of Ge on Silicon Photodetector with optical pad and MMI

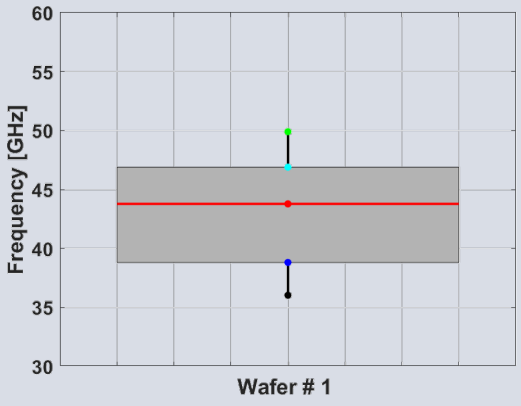
We have studied a vertical PIN Ge-photodetector of different length and width at full wafer level. All performance metrics has been evaluated. The main characteristic of the photodetector are Dark current, Responsivity, Bandwidth and current saturation. Dark current should be minimum as much as possible and Responsivity, Bandwidth and current saturation should be high as much as possible. But, there is always trade-off among these performance matrices. we can get higher Responsivity and current saturation by increasing device cross-section (upto some extend) but, as device cross-section increases, dark current increases and bandwidth decreases. We have analyzed the above performance matrices on 300 mm SOI wafer of device cross-section of 3.7 μm x 15 μm. Most of devices shows low dark current of $\sim 10nA$ and Responsivity of $\sim 0.8A/W$ at reverse bias voltage of 1V. This depend on device geometry, operating wavelength and slightly on bias voltage. we also measured saturation characteristic of this device, which show maximum current of 16 mA and 1 dB compression of $\sim 11mW$ optical power. Large bandwidth is required for high-speed data transmission. Our device shows 3 dB bandwidth of $\sim 45GHz$ at a reverse bias voltage of 1V on full wafer scale.



wafer-scale measurement result of dark current



wafer-scale measurement result of Responsivity



wafer-scale measurement result of 3-dB Bandwidth

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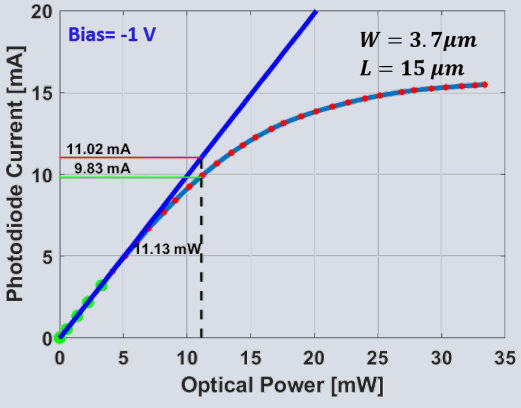


power saturation characteristics

Programmable Photonic Integrated Circuits

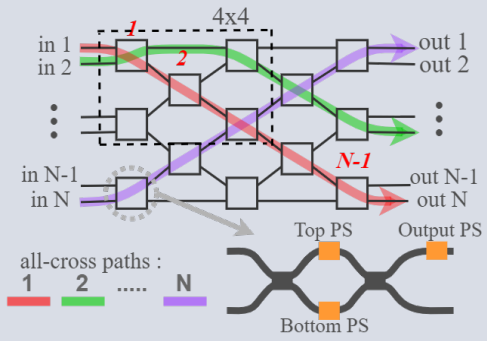
Associated Research Scholars: *Kumar Piyush, Yash Raj, Akash Shekhar, Ashitosh Velamuri, Pawan Kumar Pandit*

Silicon photonics offers various methods to actively control or program the behavior of photonic devices through external stimuli such as electrical signals and local temperature changes. Leveraging these capabilities, Programmable Photonic Integrated Circuits (PPICs) provide a highly efficient platform for rapid prototyping, enabling multifunctional, upgradeable, and software-defined solutions. These features make PPICs instrumental in advancing diverse fields, including **hardware accelerators, autonomous driving, neuromorphic computing, quantum technology, avionics, and next-generation communication systems such as 5G and beyond**.In this context, we present our recent work on three key aspects of PPICs:

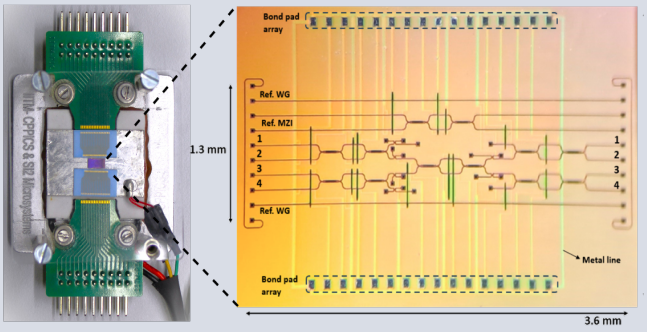
1. **Study of NxN MZI meshes in feedforward configurations**
2. **Design and analysis of a 1x4 MZI with diode-integrated metal heaters**
3. **Exploration of recirculating mesh designs using square mesh architectures**

Study of NxN MZI meshes in feedforward configurations

An $N \times N$ MZI mesh consists of $M \sim N^2$ phase-balanced MZIs, as shown in Fig. 1. Fabrication-induced waveguide variations introduce random phase errors in the MZIs. To counter these errors, correction is applied via the top or bottom phase shifter of each MZI. Efficient correction requires extracting the phase errors $(\phi_1, \ldots, \phi_M)$ before programming the mesh to achieve the desired transmission and extinction at the output ports.

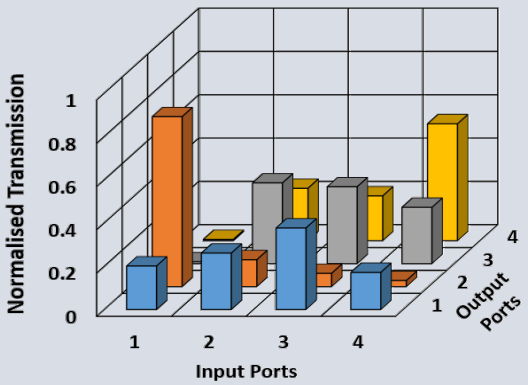


N×N MZI mesh highlighting all-cross paths, 4x4 MZI mesh (dotted), (inset) Tunable MZI structure for universal 2x2 unitary operation.

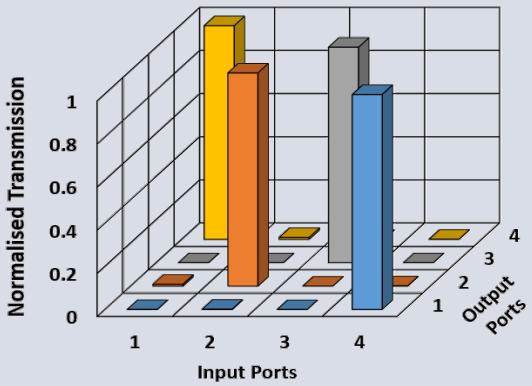


Electrically packaged 4x4 MZI mesh (consists of 5 MZIs), IMEC chip packaged at izmo Microsytems

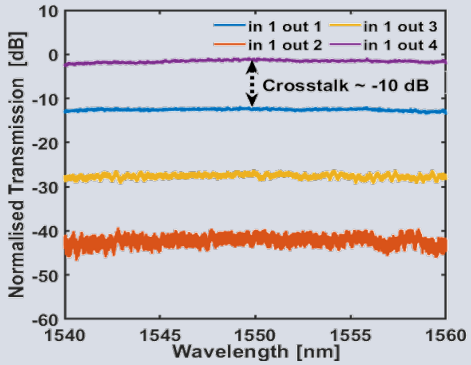
The phase errors $(\phi_1, \ldots, \phi_M)$ are extracted from measured normalized passive optical transmissions using Particle Swarm Optimization (PSO). This is achieved by minimizing the estimation error between experimental measurements and corresponding theoretical values, summed over all input-output combinations. After correcting these phase errors by applying corresponding offset power, we observed a significant reduction in optical crosstalk to -40 dB. This reduction remained consistent across all input ports throughout the



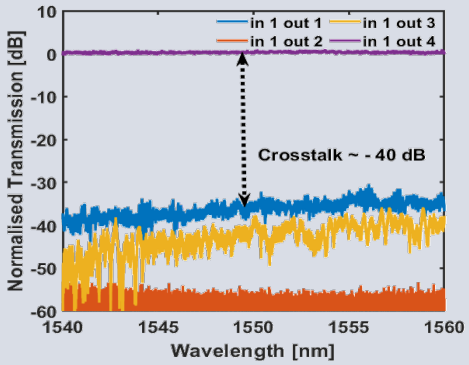
Passive transmission of simulated mesh with introduced random phase errors of a 4×4 MZI mesh



Passive transmission of simulated mesh after phase error correction using the algorithm.



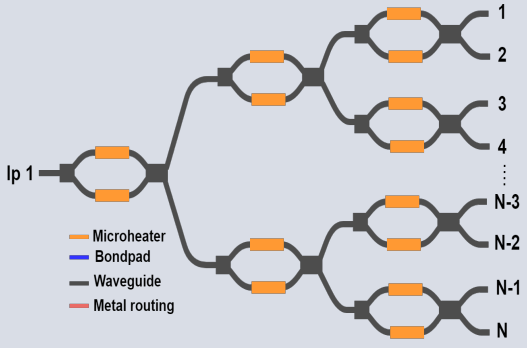
Normalized optical transmission output power of the packaged 4x4 MZI mesh upon characterization **before** phase error correction



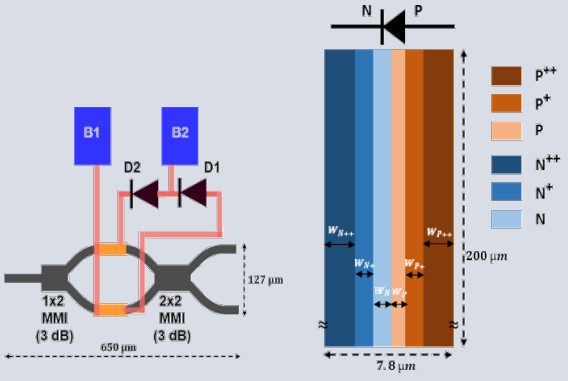
Normalized optical transmission output power of the packaged 4x4 MZI mesh upon characterization **after** phase error correction

Design and analysis of a 1x4 MZI with diode-integrated metal heaters

The 1×N programmable power splitter uses a tunable 1×2 MZI with Diode-Integrated Micro Heaters (DIMH) and two 3 dB splitters (IMEC PDK). A single bond pad enables bidirectional tuning by alternating the forward and reverse bias of the diodes.

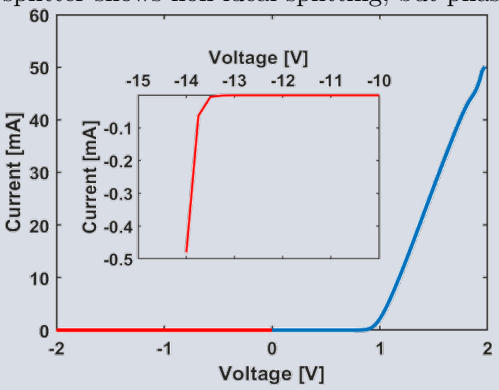


1×N power splitter design layout based on 1×2 MZIs

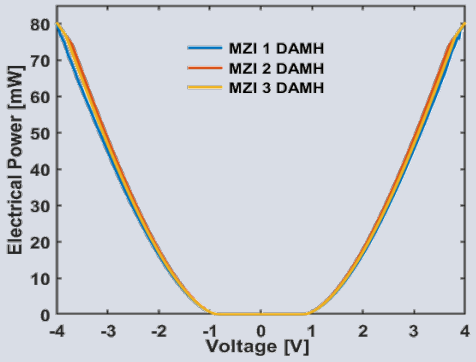


1×2 MZI scheme integrated with two diode-assisted micro-heaters and Diode design profile

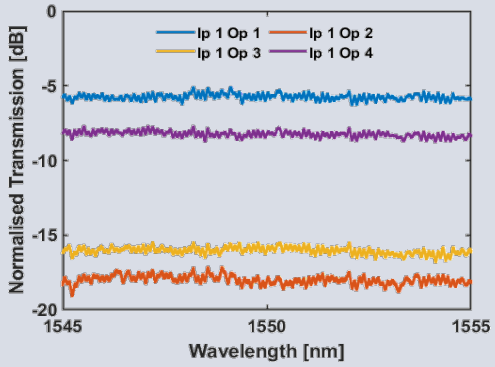
Bipolar driving for the DIMH, applying ±4V across three MZI-DIMH configurations, delivers 80 mW and reduces bond pad requirements by 50%. The normalized passive transmission for the 1×4 splitter shows non-ideal splitting, but phase correction achieves uniform splitting within ±0.25 dB.



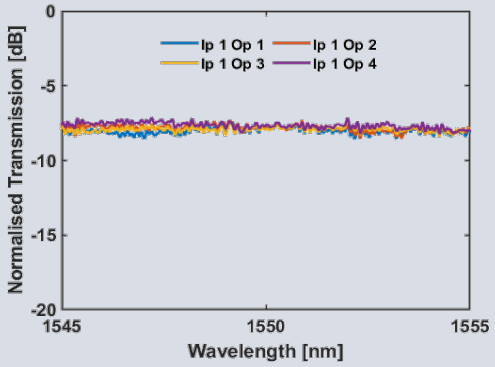
Experimental diode I-V characteristics (inset showing reverse breakdown voltage)



Electrical power delivered by Diode Assisted Metal Heater as a function of bias voltage: negative (positive) voltage for bottom (top) arm of MZIs



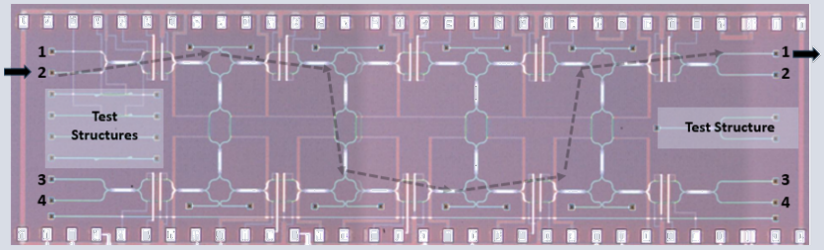
Non-uniform power splitting before phase error corrections



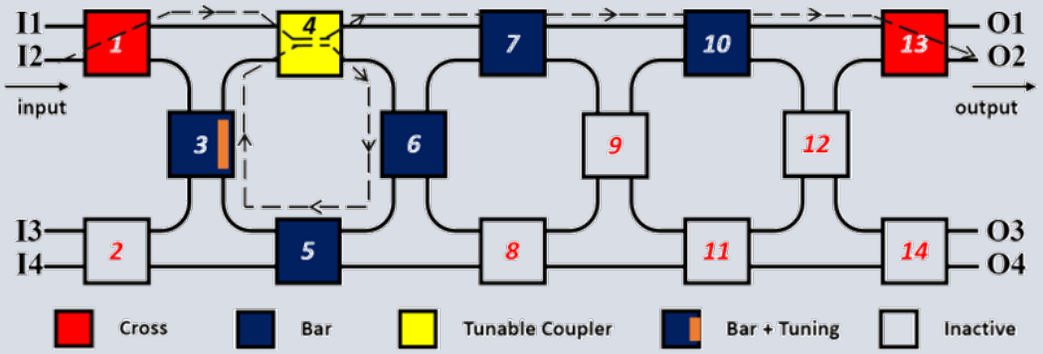
uniform power splitting characteristics after correcting phase errors

Exploration of recirculating mesh designs using square mesh architectures

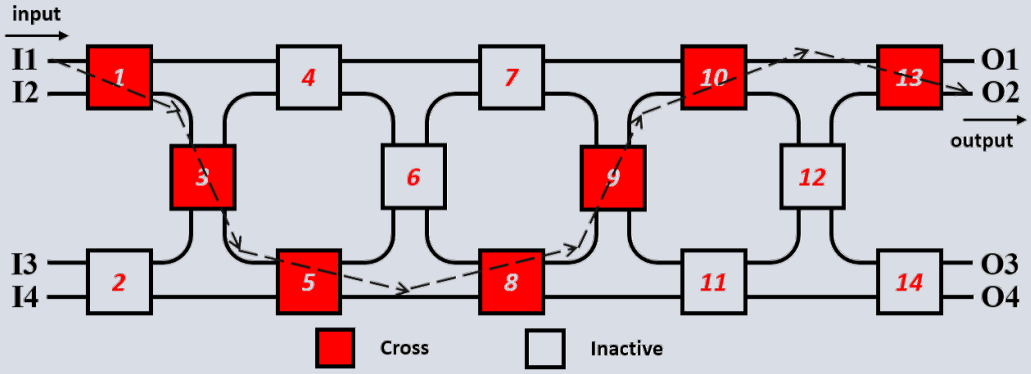
MZI-based feedforward designs are widely used for lattice filters and various photonic applications. However, realizing devices like microring resonators necessitates backward propagation, which can be achieved through a recirculating mesh architecture. To investigate this further, we fabricated a 4×4 MZI-based recirculating mesh design with tunable MZIs, enabling multiple ring configurations, one of which is depicted below. By tuning the free spectral range of the ring formed within this square mesh, we successfully demonstrated the functionality of a multiband RF filter.



4x4 square mesh, fabricated at IMEC. Arrow showing the path followed by light input at port 2 to output at port 1

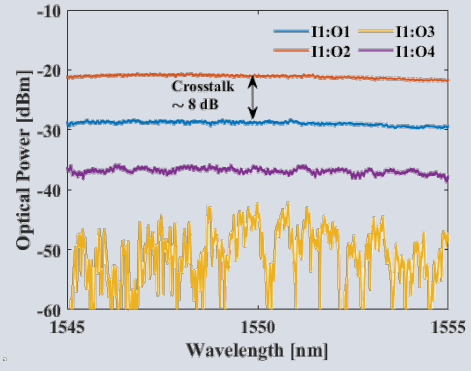


Schematic representation of the proposed PPIC to operate in a Microring Resonator configuration

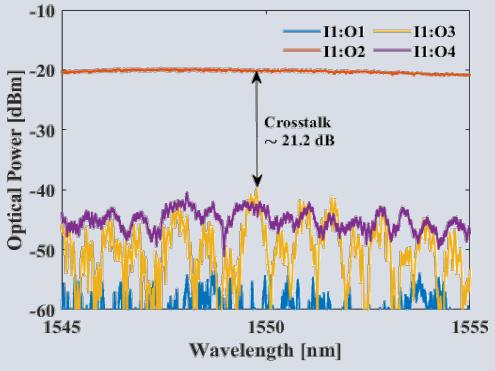


Schematic representation of the programmable square mesh indicating an all-cross path from input I1 to output O2 (I1→O2)

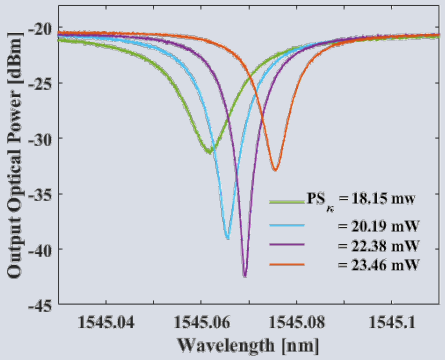
Fabrication-induced phase variations are unavoidable and can cause undesired crosstalk at the output ports. In one instance within the square mesh, with input at port 1, the initially measured crosstalk was -8 dB. After phase error correction, the crosstalk was significantly reduced to -21 dB, greatly improving the system's performance and signal quality. Following this correction, we successfully realized the ring resonator, enabling tuning of its coupling coefficient and resonance wavelength.



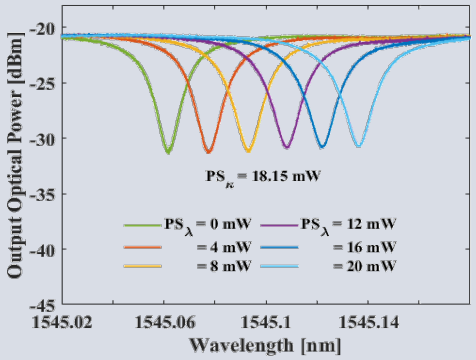
Measured optical power spectrum transmitted at the output ports before phase error corrections



Measured optical power spectrum for the selected path at all the output ports after phase error corrections

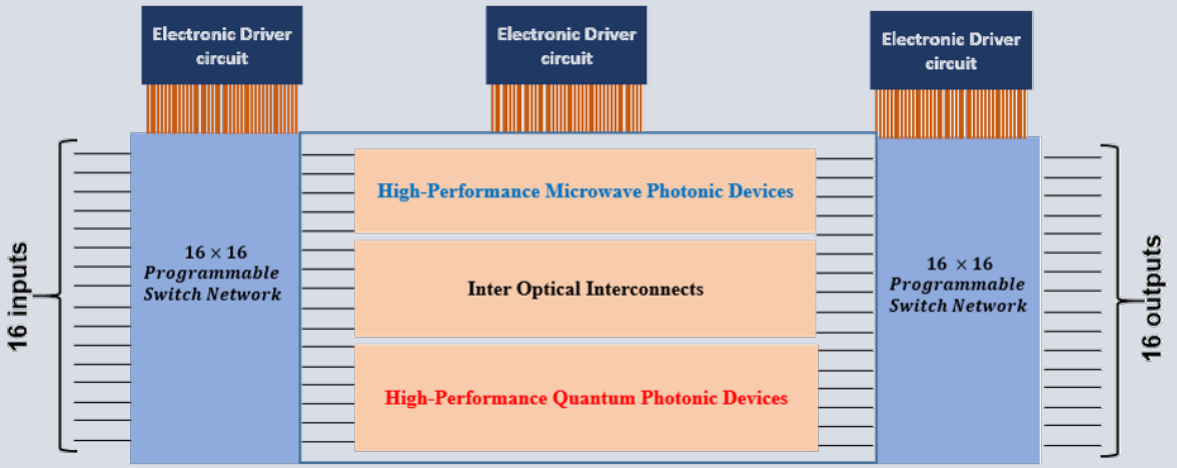


Thermo-optic tuning of MRR coupling coefficient in configuration-1



Thermo-optic resonance tuning of MRR in configuration-1 for a given coupling condition

The future of programmable photonics shows great promise, particularly in emerging fields like neuromorphic computing and computing accelerators. Neuromorphic computing seeks efficient hardware and algorithms for tasks like pattern recognition and decision-making. Programmable photonics also offers substantial potential in high-performance computing and specialized computing accelerators designed to boost specific computational tasks. Integrating specialized high-performance photonic blocks within a central hub streamlines the incorporation of one or multiple modules. This central hub, featuring an NxN input and output switch, directed by external electronic drivers, transforms into a dynamic and versatile Multipurpose Programmable Photonic Processor, catering to a wide array of functions and applications.

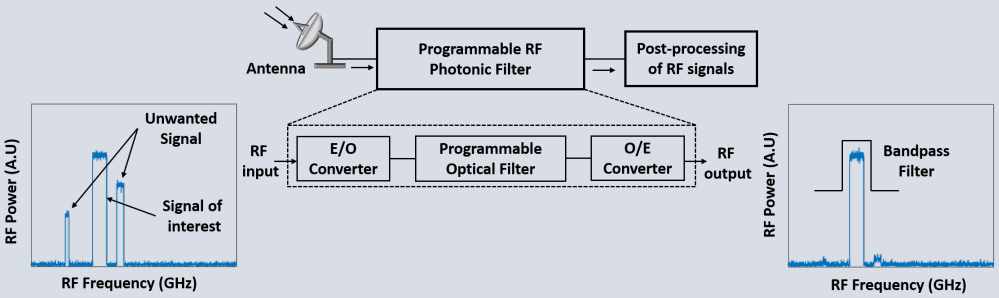


Multipurpose Programmable Photonic Processor

Programmable RF Photonic Filters

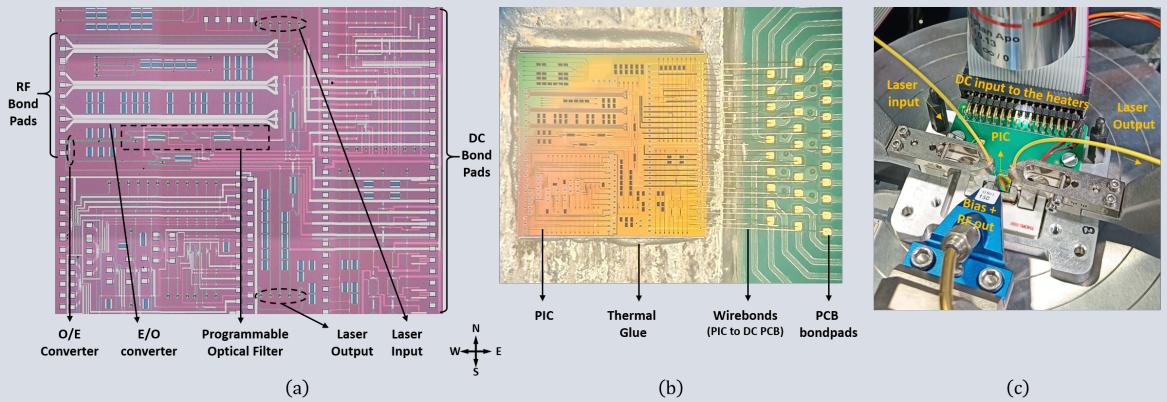
Associated Research Scholars: *Ashitosh Velamuri, Kumar Piyush and Yash Raj*

An RF filter is the basic component of any RF receiver architecture to separate the unwanted signal from the signal of interest. For this purpose, passive electrical filters are most commonly used because of their robustness and cost-effectiveness. However, these filters are designed to operate at a single frequency band with little to no scope for tuning and usually are power hungry especially at mmWave frequencies. The programmable RF photonic filters shows promise in terms of size, weight and power (SWaP), wide-band tunability and scalability, which are very crucial in 5G/6G and satellite communications and avionic applications.



General scheme of RF receiver, emphasizing the RF filter functionality.

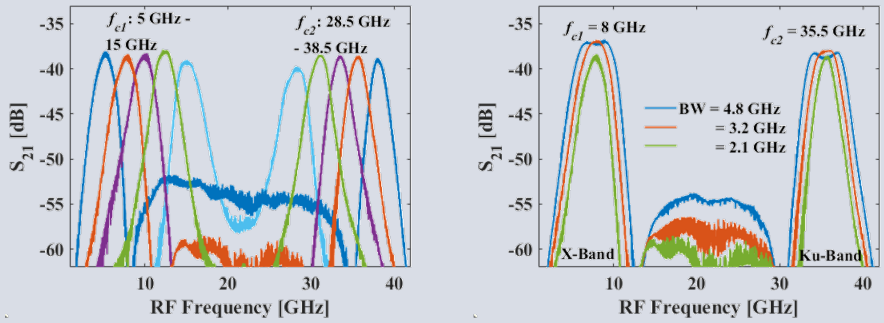
At CoE-CPPICS, we are working towards the development of a working prototype of a widely tunable (upto 40 GHz) RF photonic filter. We have proposed a novel operational scheme of the programmable optical filter to realize a tunable RF photonic filter with improved shape factor and a scope to realize multiple passband response. The photonics integrated circuit (PIC) with on-chip modulator, optical signal process and photodetector was designed at CoE-CPPICS, IIT Madras, fabricated at IMEC Belgium and electrically packaged at izmo Microsystems, Bengaluru (industry partner).



(a) (b) (c)

(a) Microscope image of the photonic integrated circuit (PIC) indicating the critical functional blocks, (b) microscope image of the PIC wirebonded to the DC PCB for multi-heater control, and (c) electrically packaged PIC probed with necessary optical, DC and RF connections during the experiment.

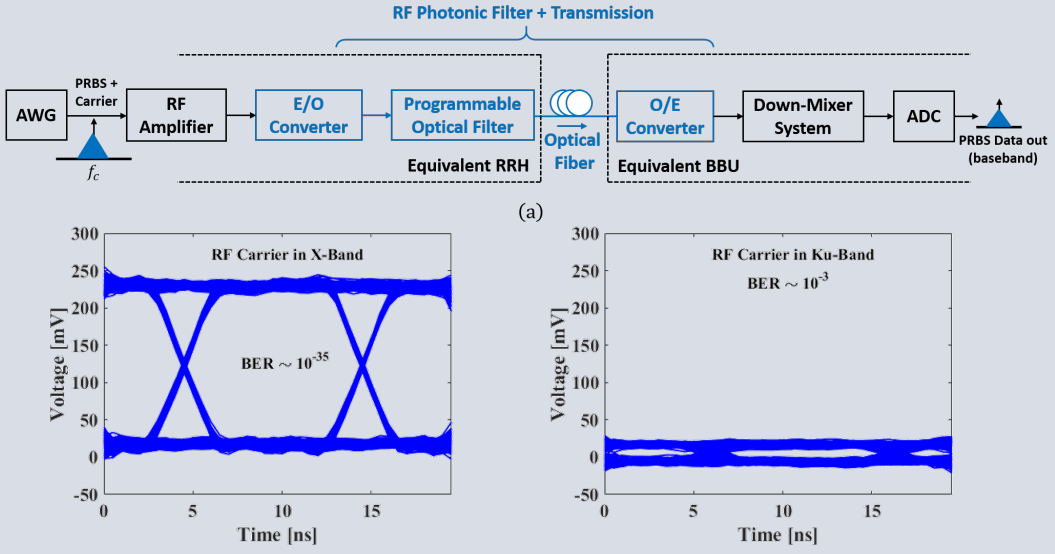
With the packaged PIC, a lab-level demonstration of the microwave photonic filter with two tunable passbands (5 GHz to 15 GHz and 28.5 GHz to 38.5 GHz)and a tunable bandwidth (2.1 GHz to 4.8 GHz) was done. For the full demonstration of the programmable microwave photonic filter, an RF interfacing printed circuit board (PCB) is critical block to feed-in and feed-out the signal from the filter module, which is currently a work in progress at CoE-CPPICS.



(a) (b)

(a) Tunable two-band RF filter over 5 GHz - 15 GHz and 28.5 GHz - 38.5 GHz. Bandwidth = 2 GHz, (b) RF filter with tunable bandwidth (2.1 GHz - 4.8 GHz) at 8 GHz (X-band) and 35.5 GHz (Ku-band).

Recently, we have successfully performed a proof-of-concept evaluation of the feasibility of the integration of the microwave photonic filter in the wireless communication networks. For this purpose, an X-band radio-over-fiber receiver link of a wireless communication network was set up at CoE-CPPICS and an efficient simultaneous data transmission and filtering operation was realized with an excellent bit-error-rates of 10^{-35} for the RF carrier aligned with the central frequency of the microwave photonic filter.

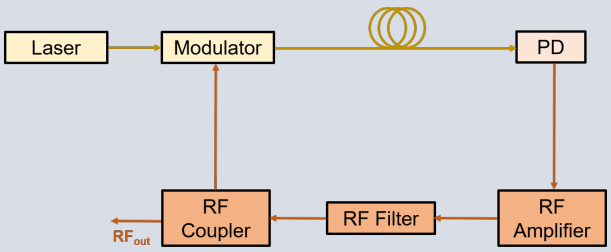


(a) Schematic representation of the programmable photonics integrated circuit (PPIC) based equivalent X-Band Radio over Fiber receiver link realized at CoE-CPPICS. AWG: arbitrary waveform generator, ADC: analog to digital converter, RRH: remote radio head and BBU: baseband unit, (b) eye diagram of transmitted data at the equivalent BBU with X-band RF carrier indicating an excellent BER of 10^{-35}, (c) (b) eye diagram of transmitted data at the equivalent BBU with Ku-band RF carrier indicating a very poor BER of 10^{-3}.

Photonic Chip based Optoelectronic Oscillator

Associated Research Scholars: *Anushka Tiwari, Ashitosh Velamuri*

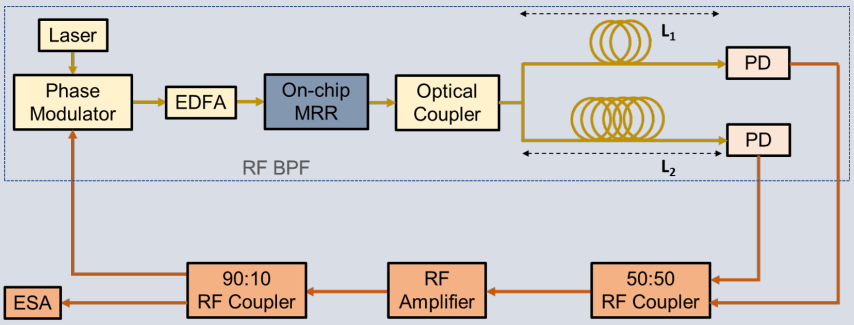
RF signal generation with low linewidth and phase noise is required in multiple applications such as radar systems, satellite communication and RF signal processing. This is mostly accomplished in bulk optics by frequency multiplication or longer low-loss delay line lengths. The optical modulated signal pass through a low loss fiber and detected in PD. Then the recovered modulated signal from the PD is amplified and pass through a bandpass filter to select frequency of operation by suppressing other cavity modes. Selected frequency of operation from RF filter is fed back to the modulator and forms an opto-electronic cavity leading to self-sustained oscillations once the loop gain exceeds the total loss of the loop. Nevertheless, optoelectronic oscillator (OEO) systems using the traditional method are large and susceptible to outside disturbances; also, a longer fiber delay line length produces a large number of closely spaced eigenmodes. It is challenging to find an electrical filter with these crucial narrowband and tunability requirements since a narrow bandpass filter is needed to choose a single oscillator mode in order to produce a spectrally pure RF signal.



Basic scheme of OEO

The on-chip MRR using low loss waveguides offers high Q-value resonances and can be a promising alternative to realize narrowband microwave photonic filters and oscillators.
In CoE-CPPICS, we have demonstrated the narrowband RF photonic filter using high-Q MRR and the RF signal generation leveraging the same optical filter on silicon nitride platform. The SMSR of the signal generated is dependent on the filter bandwidth or FSR of the generated cavity modes. Hence, to achieve high SMSR ultra narrow band filter is needed or wider FSR of the cavity modes which depends on loop length with major contribution from fiber length used in loop.

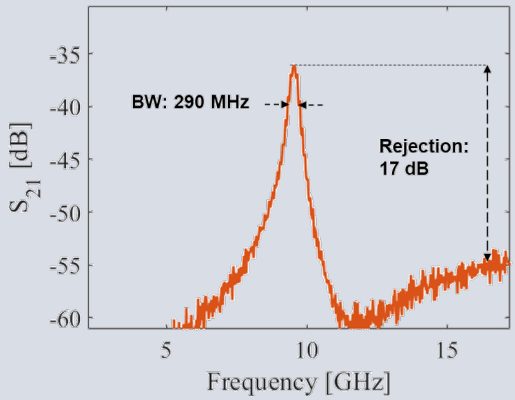
Therefore, to further enhance the SMSR and to enable single-mode selection, signal generation using a dual loop cavity has been demonstrated recently.



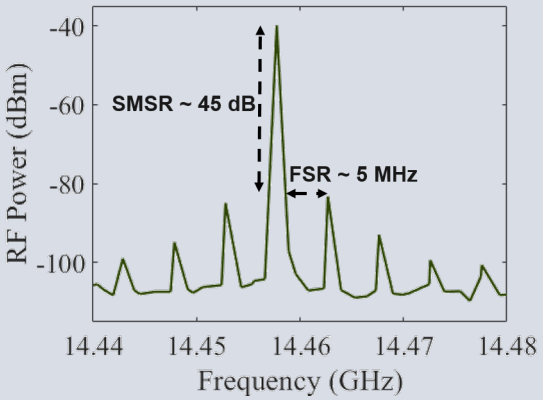
OEO scheme with integrated MRR and dual loop

In this scheme, RF signal is generated and filtered in the optical domain from the transient RF noise and looped back in electrical domain to the modulator. The central frequency of optical filter is decided from the difference between the laser wavelength (positioned near one of the resonances)

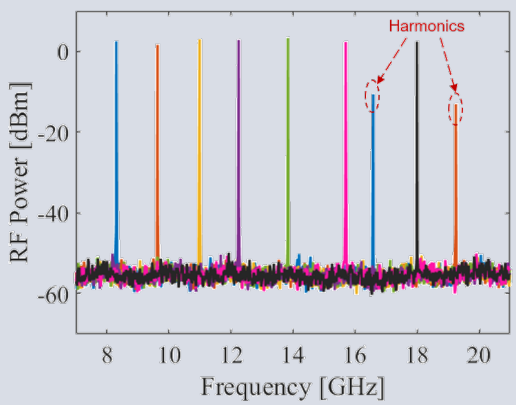
and corresponding MRR resonance which would be phase matched peak frequency of oscillation for individual loops. We have designed and demonstrated low loss waveguides based high-Q ($\simeq$ 1.7 million) MRR on SiN platform using the in-house fabrication facilities of Centre for NEMS and Nanophotonics (CNNP), IIT Madras.



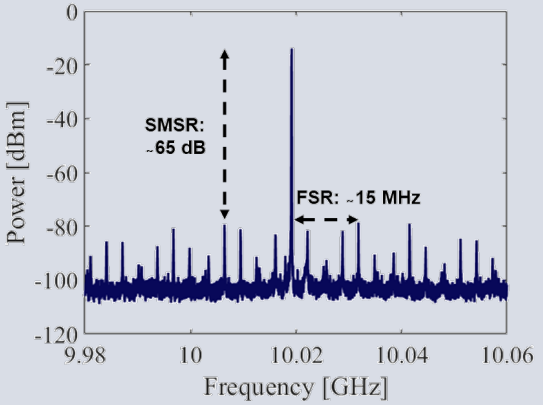
Optical bandpass filter response using MRR



Electrical spectrum of OEO generated signal



Tuning of OEO generated signal



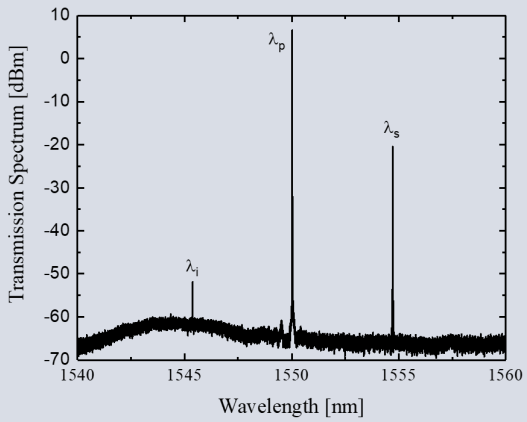
OEO generated signals for dual loop

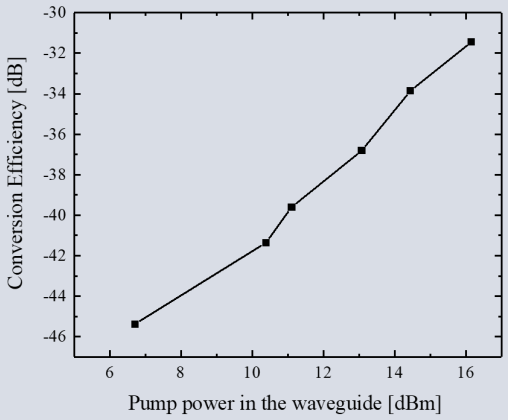
The fabricated MRR was further used to demonstrate tunable microwave photonic bandpass filters and oscillators. The observed filter response exhibits a minimum 3-dB pass bandwidth of $\sim$ 290 MHz with link gain of -35 dB. Using the narrow bandpass filter we have demonstrated microwave photonic oscillator which could be tunable upto 60 GHz (limited by the bandwidth of RF amplifier i.e. 20 GHz used in the experimental setup). Longitudinal cavity modes of the OEO have been resolved to measure the side mode suppression ratio of 45 dB with FSR of the cavity is 5 MHz.
Experiment has been further extended to increase the SMSR and FSR of the cavity using dual loop OEO. Two different fiber length is used for vernier effect where the frequency of oscillation and its FSR is decided by phase matched cavity modes in two loops. SMSR and FSR of the demonstrated dual loop OEO cavity is $\sim$ 65 dB and $\sim$ 15 MHz, respectively.

Nonlinear Integrated Photonics

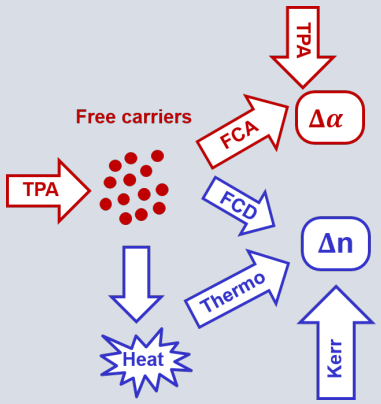
Associated Research Scholars: *Arnab Goswami, Anushka Tiwari, Pranita Ku. Swain, Nagarajan Nallusamy*

The distinctive attributes of nonlinear optical effects find practical utility within miniaturized photonic devices, enabling the manipulation of light in innovative and potent ways. CMOS-compatible integrated photonics holds significant promise across a spectrum of applications, including on-chip wavelength conversion, all-optical signal processing, parametric amplifiers, frequency combs, and photon pair generation. Our primary focus lies in utilizing four-wave mixing (FWM) for wavelength conversion in silicon and silicon nitride-based devices. Currently, we are actively engaged in research aimed at generating photon pairs and frequency combs within these integrated material platforms. The below figures illustrate the FWM spectrum and conversion efficiency in a 2 mm long silicon waveguide.





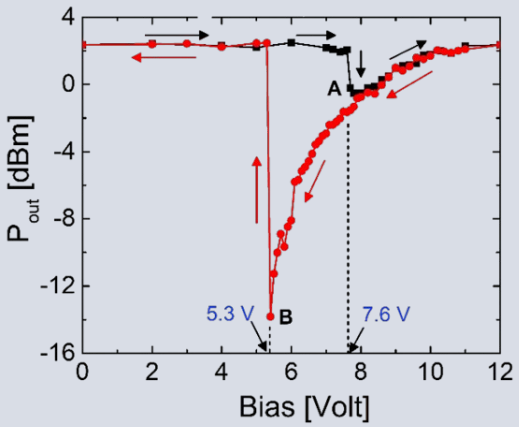
Compact microring resonator (MRR) with a suitably designed waveguide core in SOI substrate is an excellent device to enhance the field strength of a pump laser light for FWM based process. Nevertheless, optimizing silicon waveguides presents certain challenges, especially optical bistability due to self-phase modulation caused by the Kerr effect and mitigating the impact of two-photon absorption at communication wavelengths. This absorption subsequently leads to free carrier-induced plasma dispersion, making it crucial to address these issues to precisely control the strength of the pump field at resonance wavelengths with the phase shifter incorporated MRR.

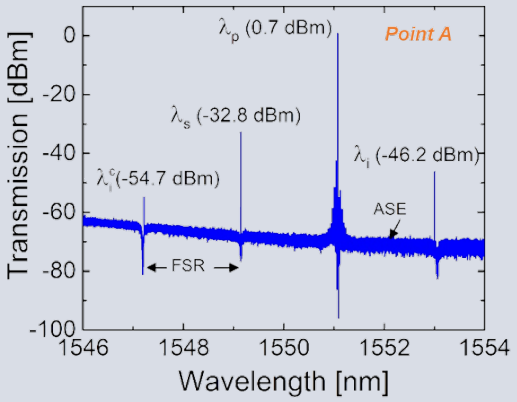


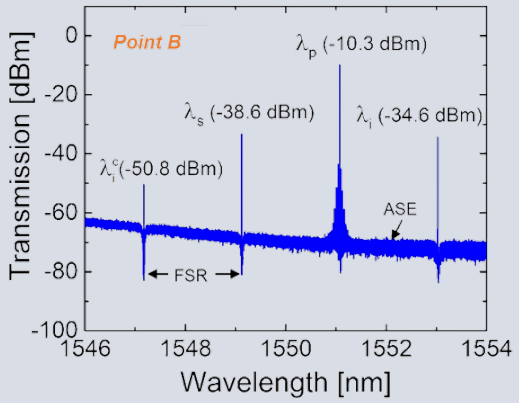
Non-linear mechanisms at high power in silicon

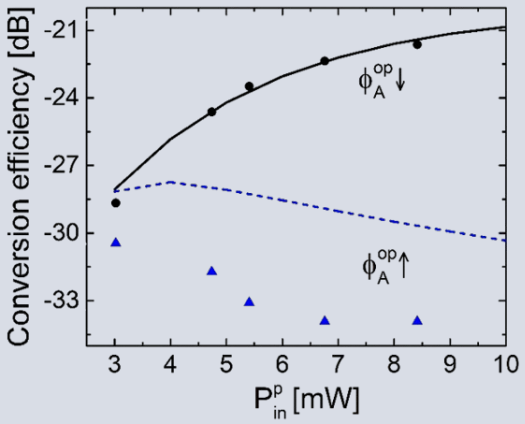
For a microring resonator of radius 50 μm, an improved stimulated FWM gain of $\sim$ 11.6 dB has been observed while thermo-optically blue-shifting resonances (point B) in comparison to that of

red-shifting resonances (point A), for a launched pump power of 8.4 mW operating at a slightly off-resonant wavelength λ_p.

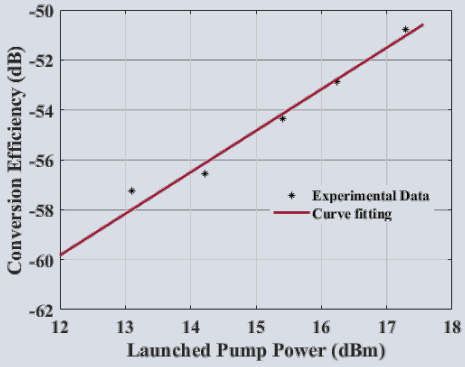








The combination of the absence of two-photon absorption (TPA) and minimal waveguide losses in silicon nitride-based waveguides equips them to withstand high optical powers without succumbing to the adverse effects of TPA. We have successfully demonstrated stimulated FWM in an in-house developed silicon nitride device with a device layer thickness of 400 nm and a device length of 2 mm. Besides, we are actively exploring its applications for photon pair generation, frequency comb generation and nonlinear optical processes, utilizing our in-house technology.



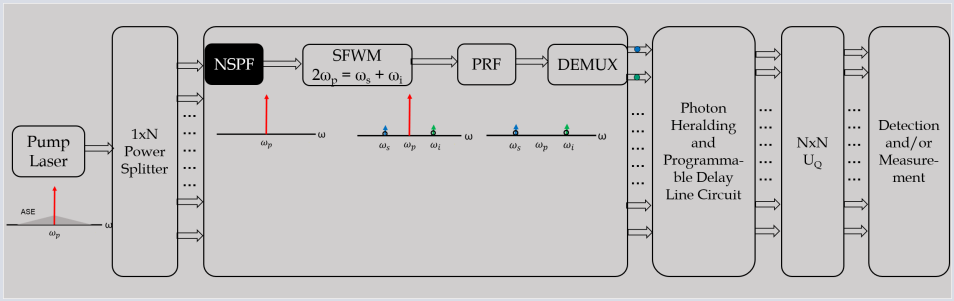
Conversion efficiency of FWM in SiN waveguide

Currently, our focus lies in generating frequency combs through the utilization of low-loss waveguide-based microring resonators. These combs offer a comprehensive spectrum of evenly spaced optical frequencies, thereby enabling precision measurements, spectroscopic applications, and the calibration of optical clocks.

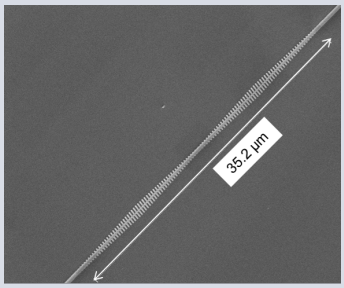
Components for Chip-Scale Quantum Photonic Processor

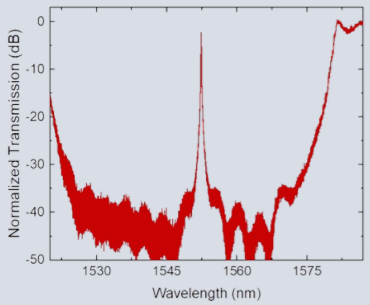
Associated Research Scholars: *Arnab Goswami, Pratyasha Priyadarshini, Ram Mohan Rao Boyapati*

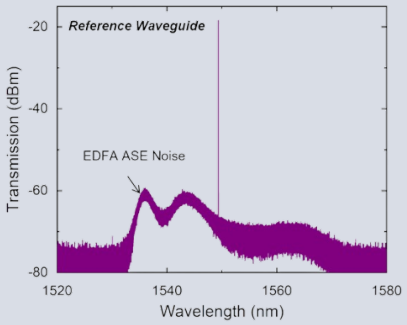
Photon pair generation through spontaneous four-wave mixing (SFWM) in silicon waveguides or microring resonators stands as a pivotal requirement in the realm of large-scale integrated quantum photonics. Nonetheless, it is crucial to employ a noise suppressed pump filter (NSPF) to mitigate the introduction of noise within the photon pair generation band. Due to the inherent challenge of modest conversion efficiency, it is imperative to promptly filter or attenuate the surplus unused pump light with pump rejection filter (PRF) by over 100 dB to avoid any noise to the originally created photon pairs along the path. Consequently, a fully integrated quantum photonic processor necessitates the inclusion of both these filter types as shown in below figure.

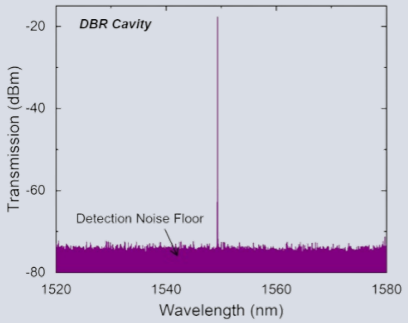


A design of compact DBR resonators ($\sim$ 40 μm-long) integrated into SOI rib waveguide structure has been demonstrated, exhibiting a resonance bandwidth as low as 40 pm ($\lambda_r \sim 1550$ nm) with an extinction of $\sim$ 35 dB over a rejection band of $\sim$ 60 nm. The device is shown to be effective in ASE noise suppression of an amplified pump laser.

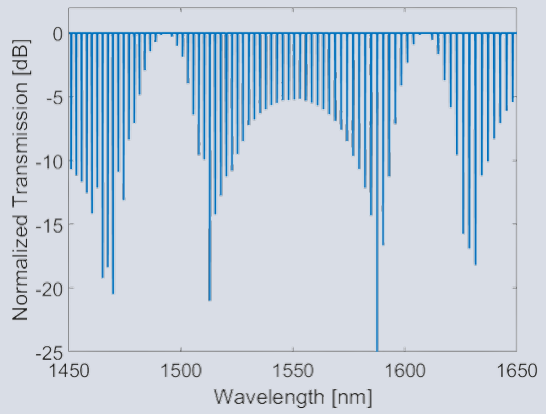


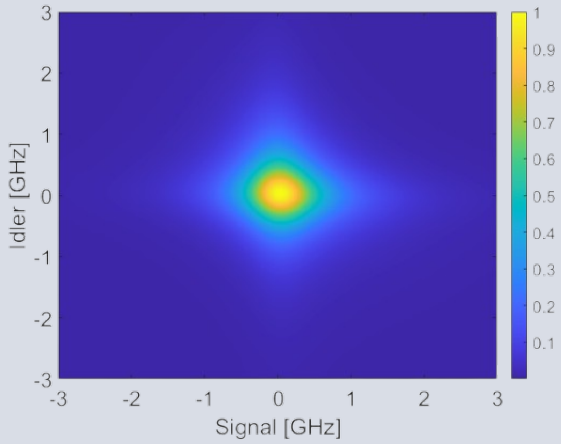




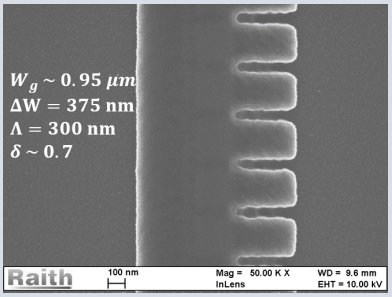


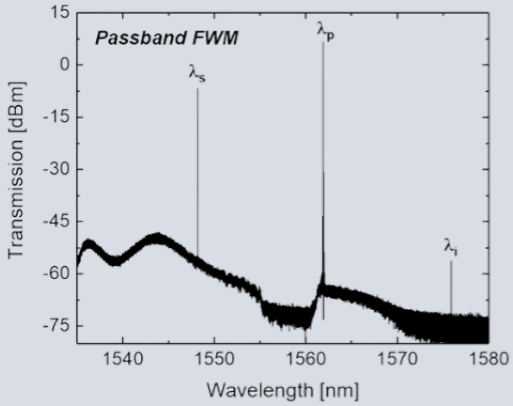
For single photon source, it is crucial, that these photon pairs remain entirely unentangled to produce heralded photons in spectrally pure states. This purity is instrumental in achieving high visibility in quantum interference. An MRR with a novel design of directional coupler can overcome the traditional purity limitation of $\sim 93\%$ and achieve purity up to $\sim 99\%$, depending on the choice of photon pairs around 1550 nm.

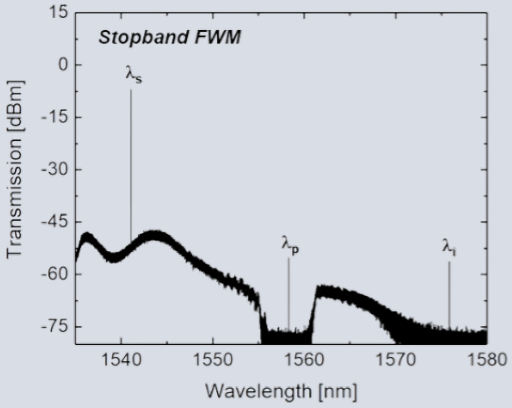




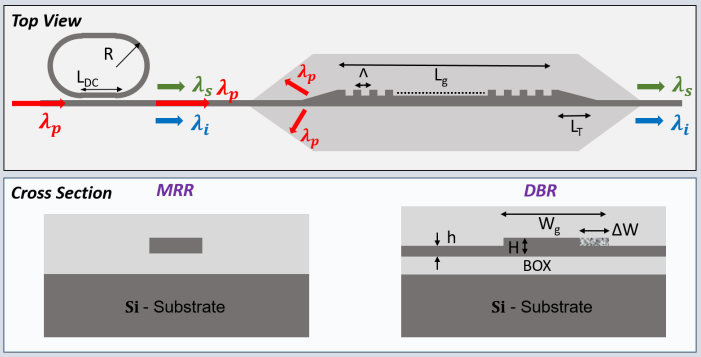
We have designed a DBR based stop-band filter around phase-matched Bragg wavelength of λ_B ~1550 nm in a multimode rib waveguide section such that the photon pair source is protected from back reflected pump. We demonstrated on-chip pump rejection of > 63 dB for stimulated four wave mixing experiment using a single stage DBR filter of length 450 μm.





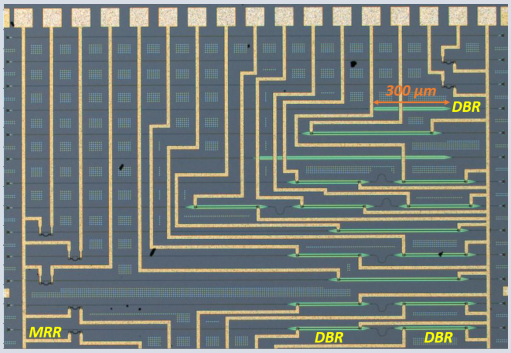


The integration of ASE filters, photon sources, and pump rejection filters represents a significant step toward realizing noise-free quantum photonic sources. The scheme for the pump suppressed photon pair generation is shown in below figure where the photon pairs are produced in MRR and followed by the pump rejection in DBR. The DBR is designed such that the reflected pump comes back with

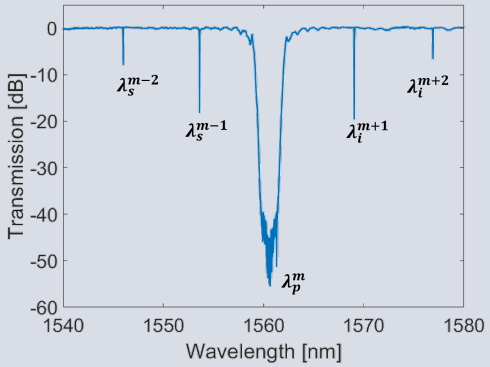


Photon source with integrated pump rejection filter

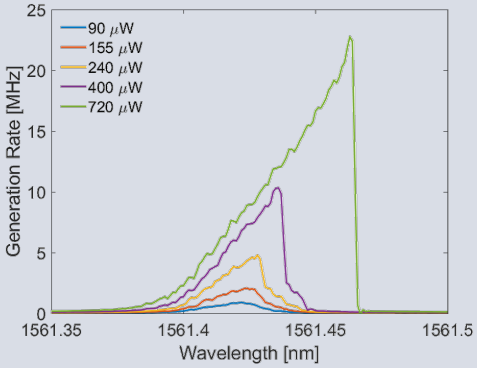
higher order mode and gets radiated which helps to prevent the source from any kind of reflection from DBR. Microscopic image and transmission characteristics of MRR with DBR have been displayed in below figures. The photon generation rate around (m-1)th has been recorded for different pump power and at higher power bistable photon generation rate has been observed.



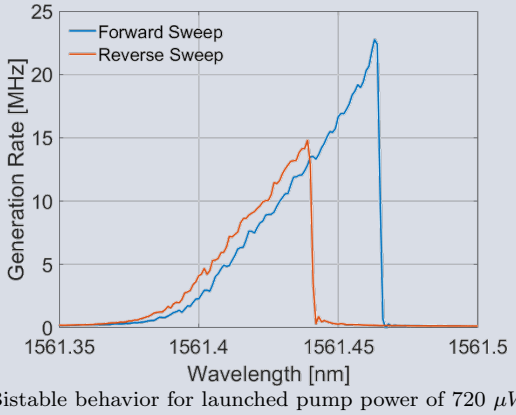
Microscopic image of fabricated chip



Normalized transmission spectrum



Photon generation across pump wavelength



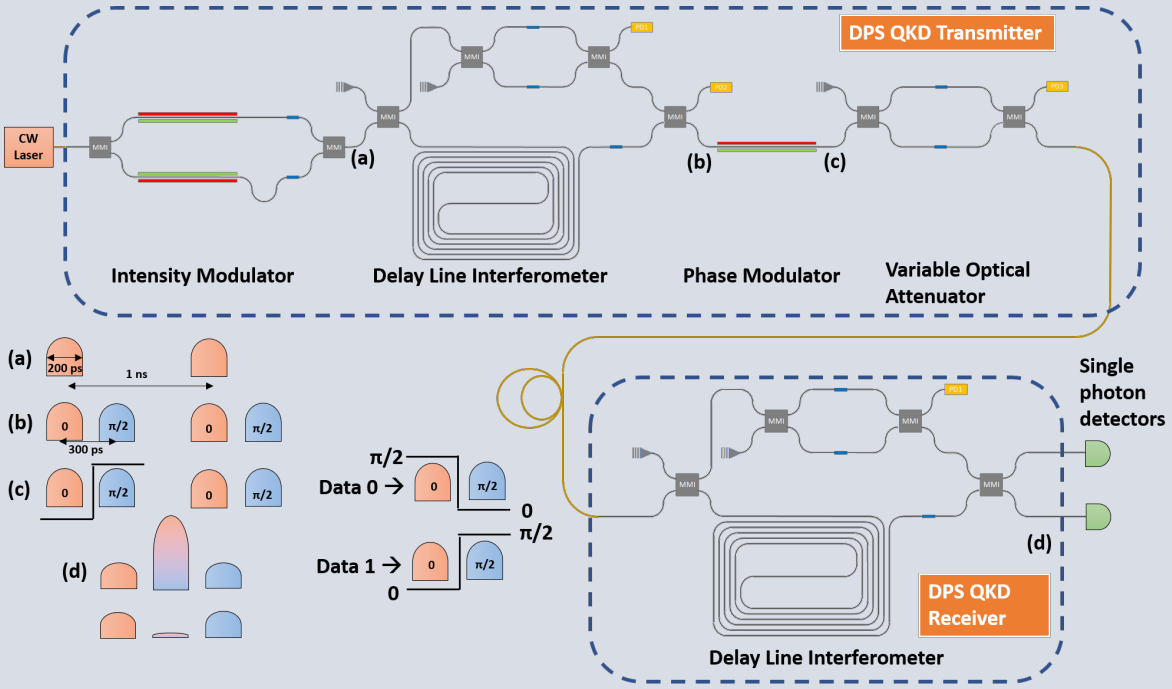
Bistable behavior for launched pump power of 720 μW

The ongoing efforts to optimize photon pair generation rate, second-order coherence, and the accidental-to-coincidental ratio promise to bring us closer to the realization of advanced quantum technologies in a large-scale photonic integrated circuits.

Chip-Scale Quantum Key Distribution Transceiver

Associated Research Scholars: *Ram Mohan Rao Boyapati, Suvarna Parvathy, Arnab Goswami, Yash Raj*

Classical cryptography depends on the time complexity of a mathematical problem such as the factorization of the product of two large prime numbers. But with the help of Shor's algorithm, quantum computers can solve the factorization problem in less time which is a huge threat to security. However, quantum key distribution uses quantum mechanics to ensure unconditional security. Practical implementation of QKD protocols based on bulk optics has been shown. Bulk optics-based QKD implementations occupy large space and also faces stability issues. Implementation of QKD on chip offers compact size, high stability, and robustness.



Design of DPS QKD on chip

We have designed an on-chip Differential Phase Shift (DPS) QKD circuit and given it for tape-out. The information in the DPS QKD protocol is the phase difference between the two consecutive pulses. The continuous wave laser is launched into the chip using an edge coupler. The intensity modulator is used for making pulses of 200 ps pulse width and repetition rate of 1 ns. The pulses pass through the delay line interferometer to make two pulses with a delay of 300 ps and a phase difference of $\pi/2$. The MZI in the upper arm of the delay line interferometer is used as a variable optical attenuator to match the power of two pulses. The phase modulator is used for modulating information on the pulses depending on the data. If the data is zero the first pulse gets $\pi/2$ phase and the second pulse gets 0 phase whereas if the data is 1 the first pulse gets 0 phase and the second pulse gets $\pi/2$ phase. At the end, variable optical attenuator (VOA) is used to attenuate the pulses to a single photon level.

At the receiver side, a similar DLI is used to extract the data by interference. There are three time windows at the receiver i.e. the early time window, the interfering time window, and the late time window. The photon detection in early and late timestamps are discarded whereas in interfering timestamp, each of the single-photon detectors get clicked depending on the data. Once the receiver gets the data, the transmitter and the receiver do the error correction and privacy amplification to obtain the secure key.
We have got a chip from IMEC ISIPP50G MPW run and characterized individual devices such as intensity modulator, delay line interferometer, phase modulator, and variable optical attenuator.

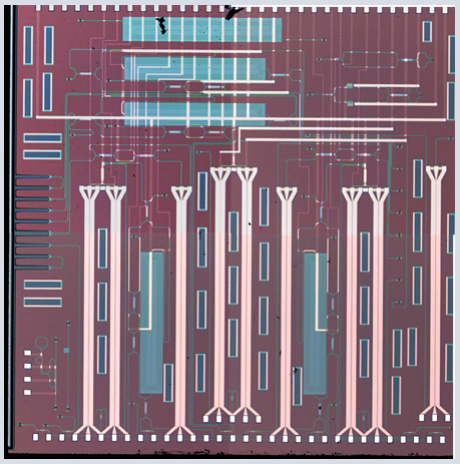
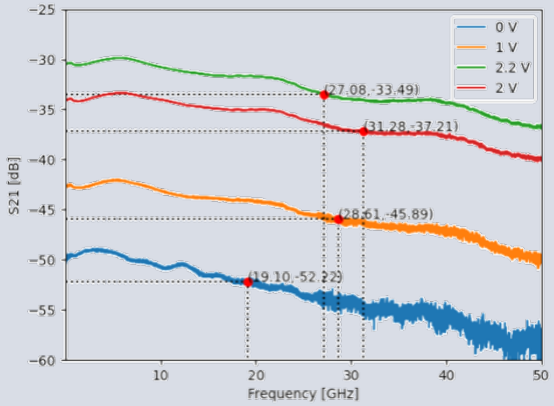
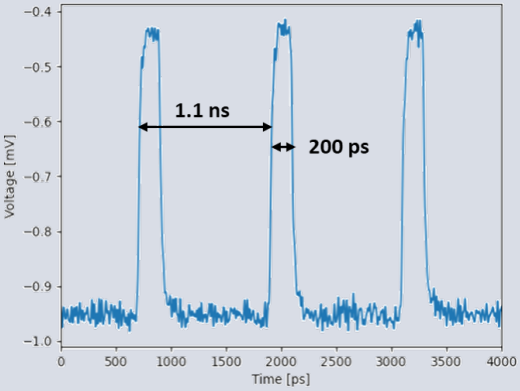


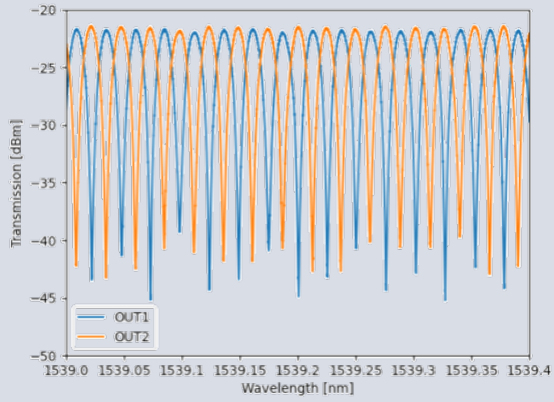
Image of DPS QKD transceiver taped-out of IMEC Belgium.



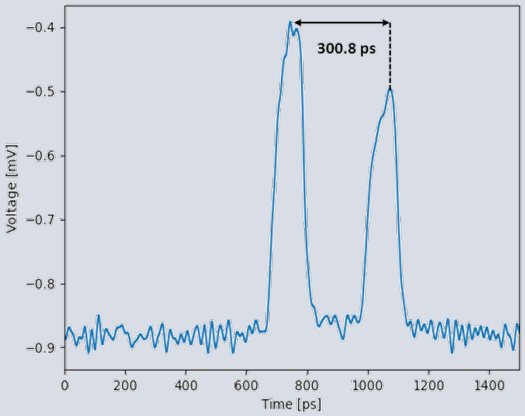
Electro-optic bandwidth of intensity modulator for different bias voltages



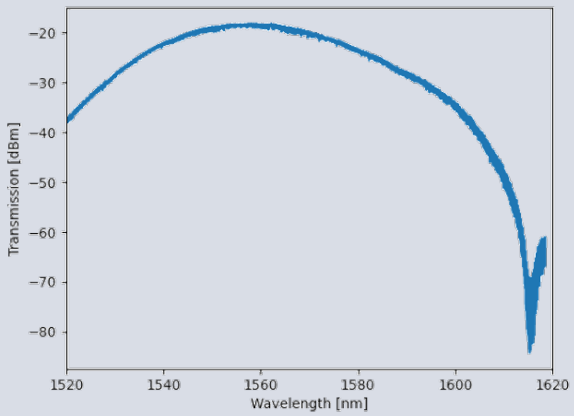
Optical pulses from intensity modulator



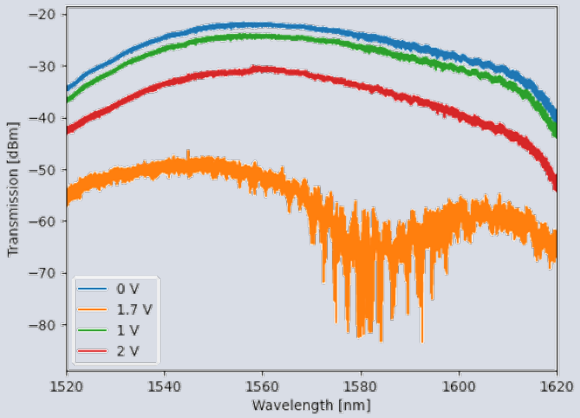
Optical transmission of delay line interferometer at two output ports



Two pulses with 300 ps delay are generated by passing a single optical pulse in delay line interferometer

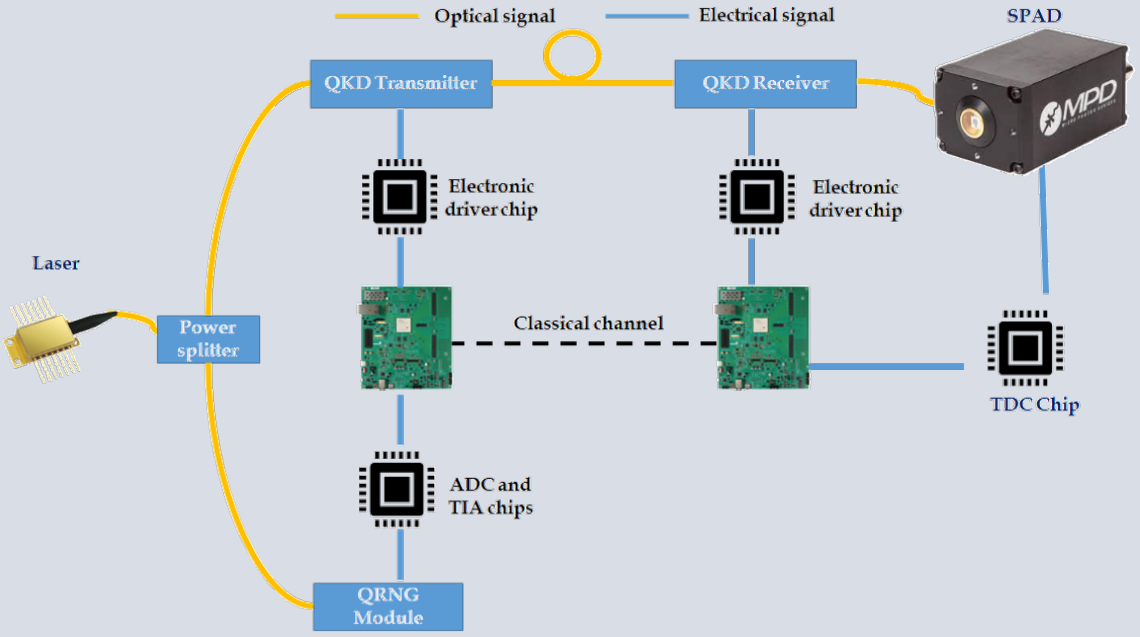


Optical transmission of phase modulator



Variable optical attenuator spectrum for different voltages

The characteristics of all the devices are as expected. We need to test the complete QKD circuit and measure the QBER of the QKD system.



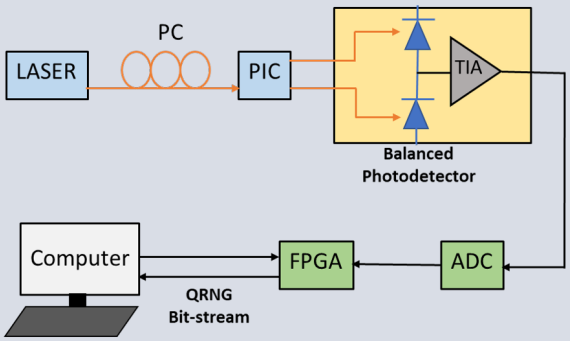
Compact QKD device with on-chip QKD transceiver and on-chip QRNG

Along with this transceiver chip at CPPICS IIT Madras, we want to demonstrate the compact QKD device with an on-chip QKD transceiver and on-chip QRNG with optically packaged and bringing the packaged electronic chips onto the same PCB board.

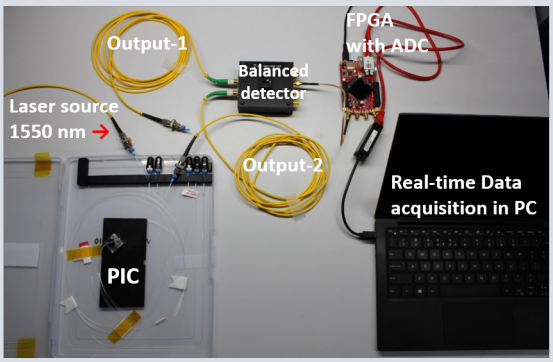
Quantum Random Number Generator

Associated Research Scholars: *Ankan Gayen, Ch.K. Siddhartha, Shamsul Hassan and Nagarajan N.*

In daily life, knowingly or unknowingly, we are using different applications of random number generators. For example, one-time password (OTP), pins provided by the bank, CAPTCHAs etc. are the outputs of a random number generator. High-quality random numbers are needed to ensure security of these transactions/communications. Among different kinds of random numbers, Pseudo random Number and physical random numbers may be predicted by quantum computer, hence cannot be usable for the case of secured communication schemes, such as classical cryptography, or quantum key distribution (QKD) protocols followed in Quantum Communication. On the other hand, true random number generators (TRNGs) harness natural, stochastic random processes as the source of randomness, hence producing extremely high quality random sequences.

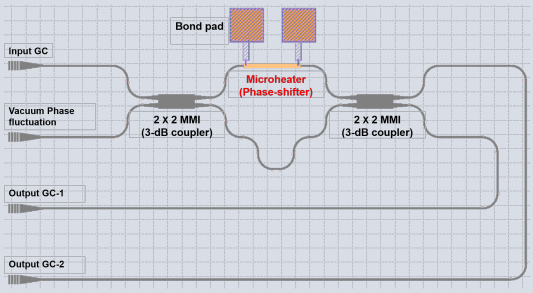


Block diagram of PIC based QRNG



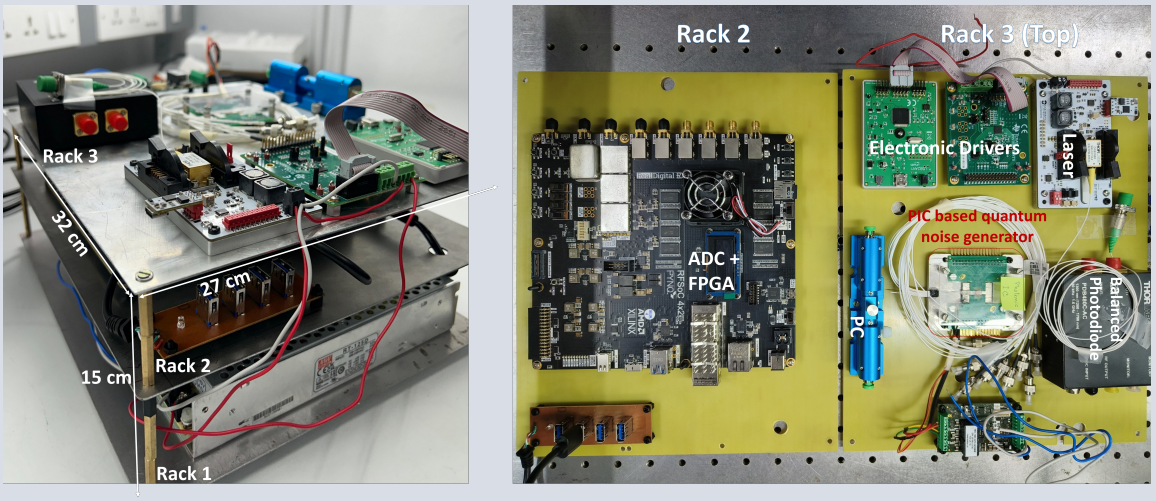
Experimental realization of QRNG

Quantum Random Number Generator (QRNG) is a type of TRNG where the source of randomness is generated from quantum-mechanics driven physics. Among various sources of entropy that exist in quantum physics, the sources present in the field of optics is capable of generating random numbers at a very high speed. We have exploited the vacuum noise fluctuation as the source of randomness in our experiment. The experimental setup is shown above, where the same source of randomness is exploited to generate real-time truly random bit streams.



PIC design layout for QRNG

The PIC design layout for QRNG is shown in left figure. It is composed of MZI structure having MMI based 3-dB splitter and phase shifter at the arm of MZI. It can be fabricated by leveraging our in-house integrated silicon photonics technology and also compatible with CMOS fabrication foundries. The corresponding experimental set-up of PIC based QRNG is already illustrated above. From Laser source, light is launched into PIC through on-chip grating coupler and polarization controller (PC) is used to enhance the power coupling efficiency by controlling the TE/TM



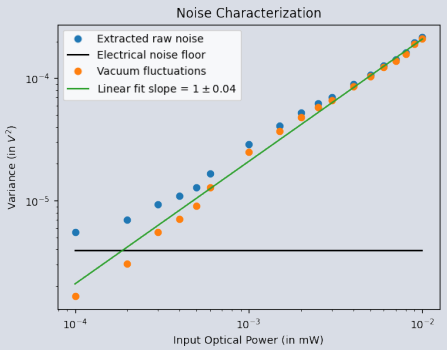
Prototype development of a standalone PIC based QRNG Module.

polarization of the light. The output of PIC is given to a balanced homodyne detector with an inbuilt Trans-Impedance Amplifier (TIA) to obtain a shot noise signal by subtracting the classical noise. The analog-to-digital converter (ADC) is used for RF signal (analog signal) to digital signal conversion and post processing is performed by FPGA to generate real-time QRNG data.

The fiber-to-photonic chip attachment has been done to perform the QRNG experiment. Here, a special type of fiber array is used for fiber-to-chip light coupling, called V-Groove Array (VGA). There, all the fibers are equispaced, and the same pitch is maintained between the Grating Couplers (GCs) on a chip so that the alignment of the extreme two optical fibers with the corresponding GCs automatically ensures the alignment of the rests. After packaging the chip, all the peripheral electronics along with the FPGA are assembled to develop a standalone QRNG module, as shown in the above figure.

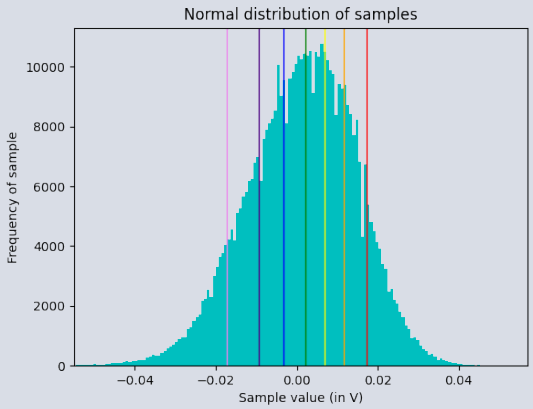
Our future plan is to integrate the photonic circuit and the balanced photodetector circuit in a monolithic CMOS compatible (SOI) platform. All the other required components for QRNG will be assembled on a single PCB board, that will drastically reduce the form factor of the module. We already demonstrated a TEC controlled and electrically packaged photonic chip which is discussed in details in the packaging section, thus proceeding towards a fully packaged Quantum Random Number Generator prototype.

The signal(raw noise) from the balanced photodetector is a collection of quantum noise and classical noise. We consider classical noise the photodetector electrical noise(noise floor) when laser power is off. The quantum vacuum fluctuations (quantum noise) increase with the laser power, as seen in the output signal's variation in the Figure. To get the maximum quantum noise to classical noise ratio, we operate in the range of 10dBm laser power.

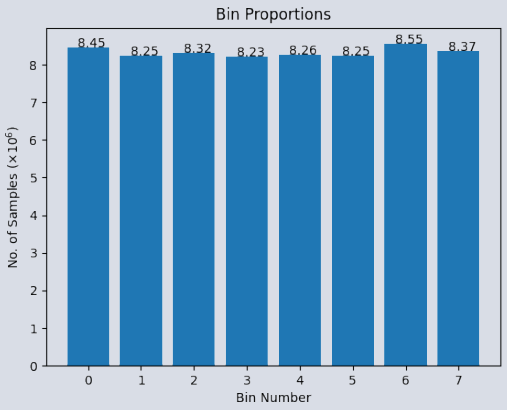


Quantum noise characterization

We use FPGA and embedded ADC to sample the noise signal (Gaussian) and categorize each sample into one of the eight bins based on its quantile, as shown in the left (Figure (a)). The quantile cuts divide the Gaussian into equal areas. The samples between adjacent quantile lines(quantile cuts) belong to a specific bin. Therefore, each bin has an almost identical number of samples, as shown in the right (Figure (b)).



(a) Noise signal with quantile cuts



(b) Uniform distribution of Bin proportions

Advantages of PIC-based QRNG

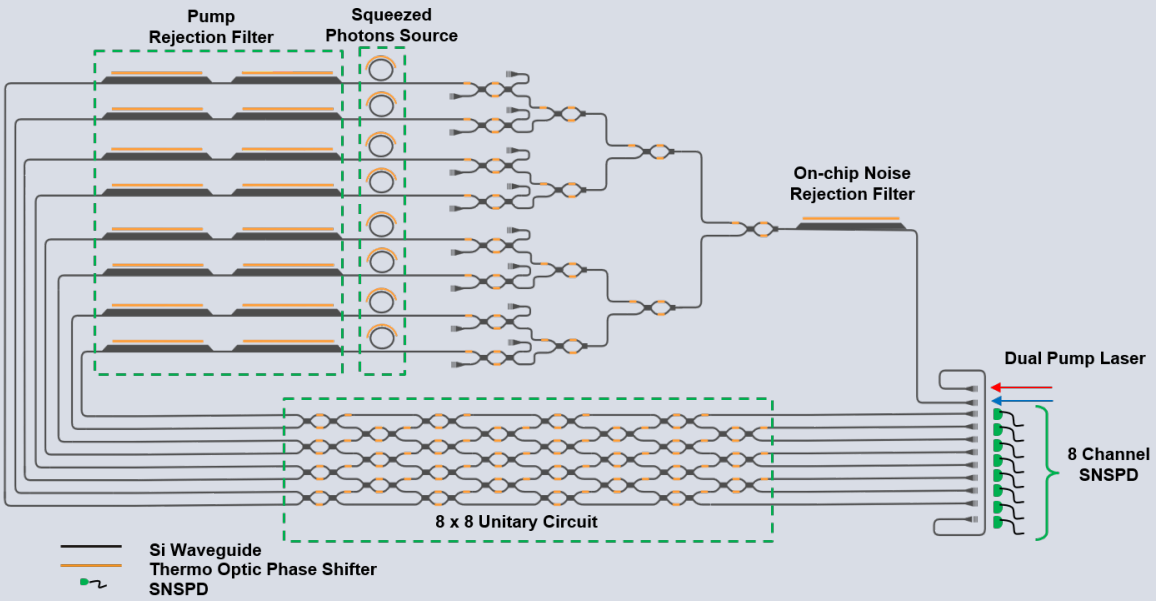
- Scalability (CMOS compatible platform)
- Low cost in mass production
- High generation rate
- High randomness due to vacuum phase fluctuation source of entropy
- High stability
- High flexibility (in terms of applications)

Applications

- Any cryptographic algorithms
- QKD transceiver
- Scientific Modelling & Simulations
- IT security for military and defence
- Financial transactions/ OTP/ Blockchain
- Gaming applications

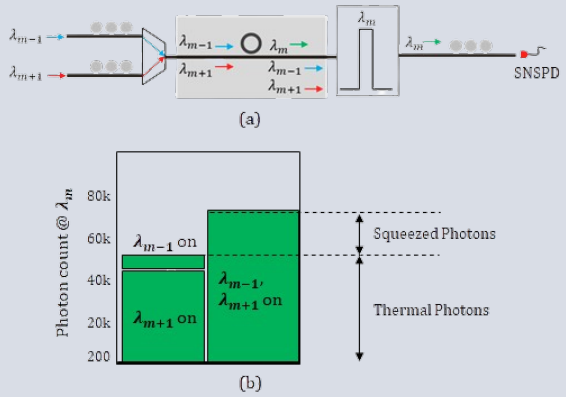
Quantum Photonic Computation

Associated Research Scholars: *Yash Raj, Ram Mohan Rao Boyapati, Arnab Goswami*



Schematic for Gaussian Boson Sampling (GBS) circuit

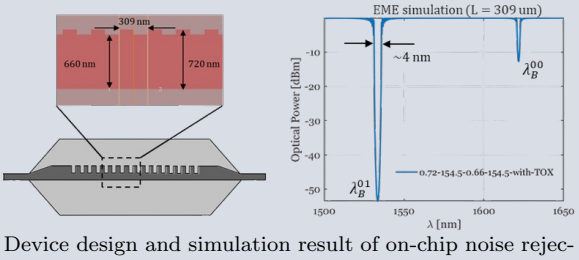
Gaussian Boson Sampling (GBS) is an important quantum experiment whose outcomes have the potential to accelerate many critical and computationally hard tasks like - graph optimization problems, drug discovery problems and cryptography. We are working towards the implementation of GBS on Silicon Photonics platform. On-chip implementation of GBS enables small footprint and feasible mass production using mature CMOS technology. The schematic diagram (above) shows the various stages in GBS, namely - on-chip noise rejection filter, optical power splitter, squeezed photon generation, pump rejection filter, quantum interferometer, and finally single photon detection. Squeezed photon is a non-classical state of photon that interfere in MZI mesh to produce photon click patterns that follow a distribution which can not be computed efficiently with a classical computer. Before squeezed photon generation on-chip noise rejection filter is critical as it removes the noisy photons in the wavelength of interest. Optical power splitter stage is used to control amount of optical power in the subsequent stage of squeezed photon source array. Pump rejection filter stage removes the pump photons from the circuit after they have been used to generate non-classical squeezed photons. We have experimentally demonstrated the on-chip pump rejection filter with stop-band extinction ratio > 65 dB for single stage, with negligible insertion loss in the pass-band. A two stage pump rejection filter is sufficient to attenuate the dual pump far below the single photon level. At this stage the the waveguides are sufficiently free from unwanted classical light. The squeezed photons enter into the unitary circuit for interference. The output photon click pattern observed in the SNSPD is governed mostly by the squeezing parameter of the incoming photons and transfer function of the unitary circuit.



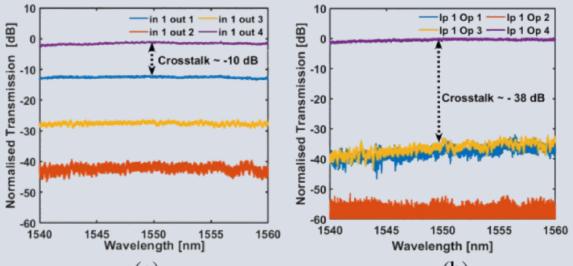
(a) Experimental setup and (b) preliminary evidence of squeezed photon sources using micro-ring resonators (MRR)

Squeezed photons are quantum photons that show noise less than the shot noise limit (SNL) along one of the quadratures of electromagnetic amplitude. On silicon photonic platform, squeezed photons can be generated using degenerate four wave mixing (FWM). The figure on the left shows the experimental setup used for preliminary evidence of degenerate FWM. Micro-ring resonator (MRR) is used to reach optical nonlinearity regime within the cavity. When photons are pumped into $(m-1)^{th}$ and $(m+1)^{th}$ resonance of the MRR, non-degenerate FWM produced photons in the m^{th} resonance of the MRR, photons produced via this process are squeezed photons.

The dual pump laser input used to produce squeezed photons may have unwanted photons in the wavelength at which squeezed photons will be produced. Therefore, it is essential to remove these unwanted photons before the dual pump is used for squeezed photon generation. The filter stop-band width must be smaller than the separation between the dual pumps and extinction in the stop-band large enough to sufficiently remove the noisy photons. The figure on the right shows the device design and simulation result of on-chip noise rejection filter.



Device design and simulation result of on-chip noise rejection filter to be used in GBS circuit.

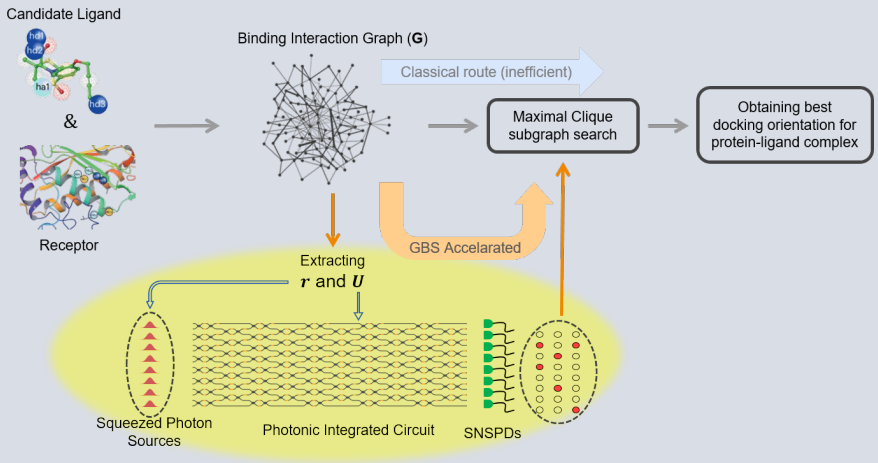


Experimental demonstration of local phase error correction and reduction of optical crosstalk at the output ports of a 4x4 unitary circuit.

Due to fabrication induced errors, the unitary circuit deviates from its ideal behaviour. However, the knowledge of actual transformation is essential to use and interpret the click patterns of the GBS experiment. We have proposed an algorithm that estimates local phase errors of MZI mesh using classical optical measurements of the unitary circuit. We have demonstrated the algorithm experimentally on a 4x4 MZI mesh. The figure on left shows the reduction in optical crosstalk (caused due to phase errors in individual MZIs of the mesh) upon implementation of our algorithm.

Target applications of GBS:

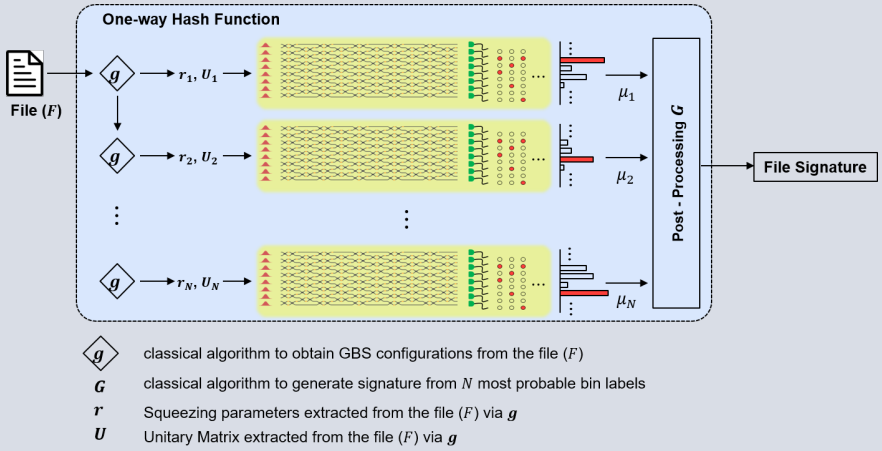
1. Drug Discovery



Major steps involved in drug discovery highlighting the acceleration possible using GBS.

Finding compatible ligands for target receptors is an important step in the drug discovery process. The step of maximal clique subgraph searching is a major bottleneck in the process. GBS accelerates the searching process by giving subgraphs biased towards the right answer.

2. One-way Hash Function Generation



Process of obtaining file signature for any given file using GBS to generate one-way hash functions.

One-way hash functions are widely used to generate digital signatures for validation of confidential files and passwords. However due to advent of quantum technologies, it may be easier to modify the files without affecting its signature, thus compromising the security. GBS can be used as of part of one-way hash function to generate signatures that may be immune to the quantum technologies.

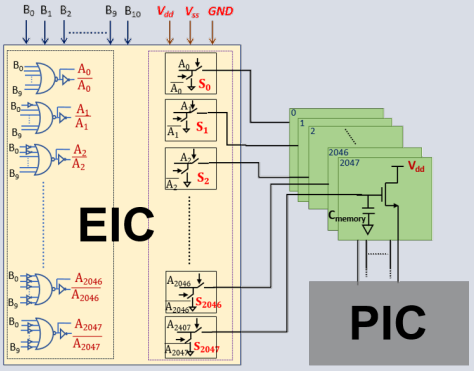
Silicon Photonics System Integration

Photonic system integration combines photonic, electronic, and thermal components of a photonic integrated circuits (PICs) using electronic-photonic co-integration and packaging. Silicon photonics integration is vital for incorporating PICs into products like optical transceivers, LiDAR systems, and optical sensors.

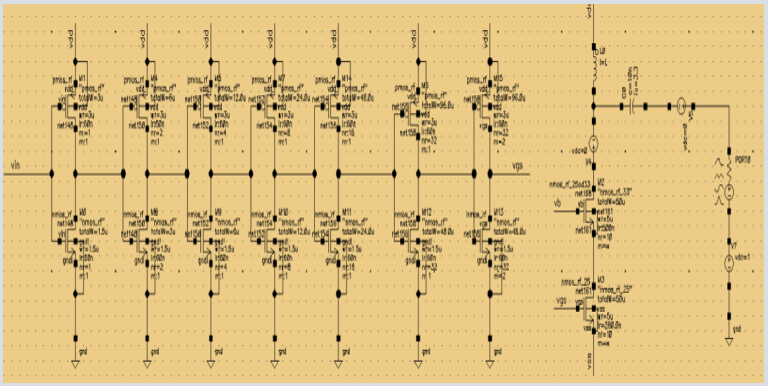
Electronic Driver for Photonics

Associated Research Scholars: *Kumar Piyush, Dibyanchal Sahu, Mayukh Mandal, Akash Shekhar, Manu Maxim, Chaganti Kamaraja Siddhartha*

Photonic system integration unites two vital technologies: electronics and photonics, merging their strengths into a single chip. Electronics can handle computational tasks efficiently but there is lag in speed and energy efficiency over long distances. Photonics, in contrast, beams data at light speed with minimal energy use. This fusion meets the need for faster, more efficient data transmission, slashing latency and interference risks. In applications like **data centers**, **telecommunications**, and **quantum computing**, where data demands are surging, electronic-photonic integration bridges the gap and unlocks the unique advantages of both technologies. Recent work focuses on designing CMOS multiplexer circuits for driving numerous phase shifters in programmable photonic integrated circuits (PPICs) using zero-change silicon photonics fabrication technology, enhancing functionality and programmability.

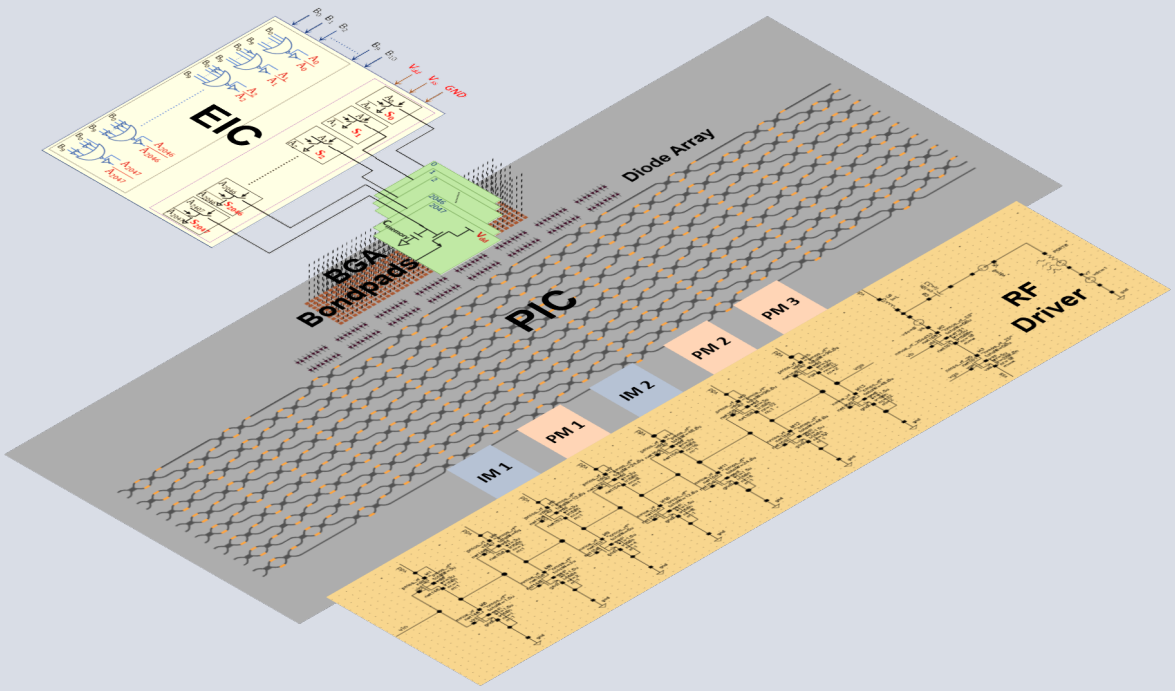


CMOS Multiplexer Design for PICs using Silicon Photonic Technology



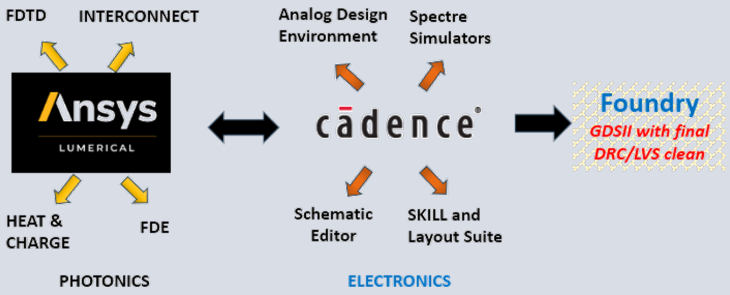
CMOS RF Driver circuit for PPICs using TSMC 65nm technology

Electronic-Photonic Co-Packaging techniques: The shift from electronic-photonic blueprints to actual production hinges on advancing fabrication and packaging methods that blend electronic and photonic elements. Diverse co-packaging techniques are there, including **Side-by-side wire bonding, 2.5D integration on an interposer, flip chip/micro pillar integration, 3-D stacking with through silicon vias, and monolithic integration.** Monolithic integration condenses everything onto a single chip but complicates design and thermal control. Flip chip bonding resolves some of these challenges but may encounter electrical and thermal interference.

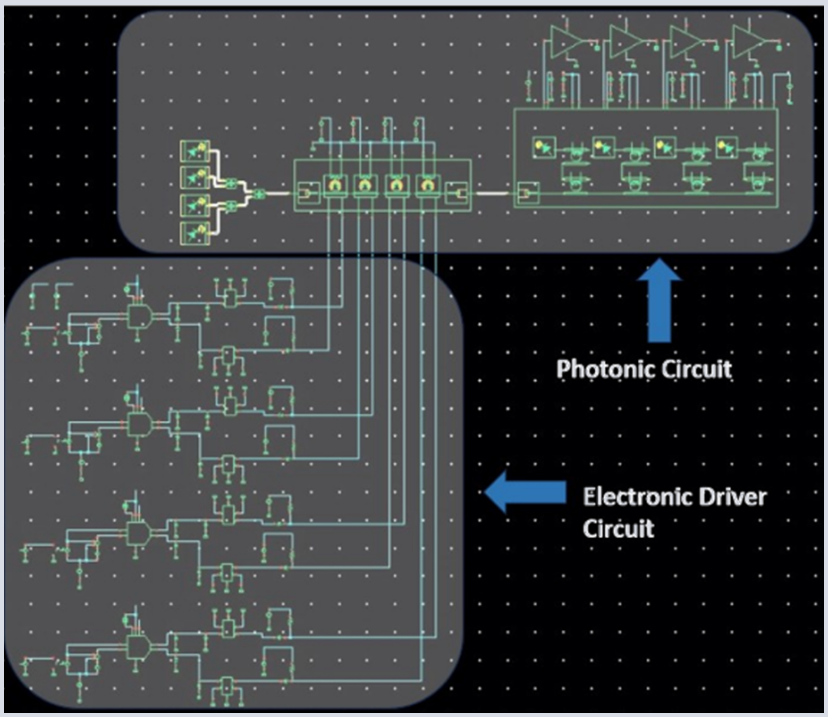


Co-integrated design of Photonic Integrated Circuits (PICs) and Electronic Integrated Circuits (EICs) using Ball Grid Array (BGA) packaging. The figure also shows the Intensity Modulator (IM) and Phase Modulator (PM) driven by an RF driver for RF circuit analysis

Electronic-Photonic Co-Design Platform: To evaluate the enhanced functionality of co-integration, a robust co-simulation platform is essential. This platform necessitates the adaptation of existing EDA tools to accommodate photonic schematics while maintaining a clear distinction between optical and electrical connections to prevent inadvertent crossovers. The Electronic Photonic Design Automation **(EPDA)** framework facilitates designers in schematic capture, circuit simulation, and schematic-driven layout. It also extends support for complex photonic p-cells and advanced photonic layout generators, enabling seamless integration of photonic and electronic systems. Prominent industry leaders in this domain include **Cadence, GlobalFoundries, Ansys, Synopsys, and AIM Photonics**, driving innovation in EPDA solutions for next-generation photonic technologies.

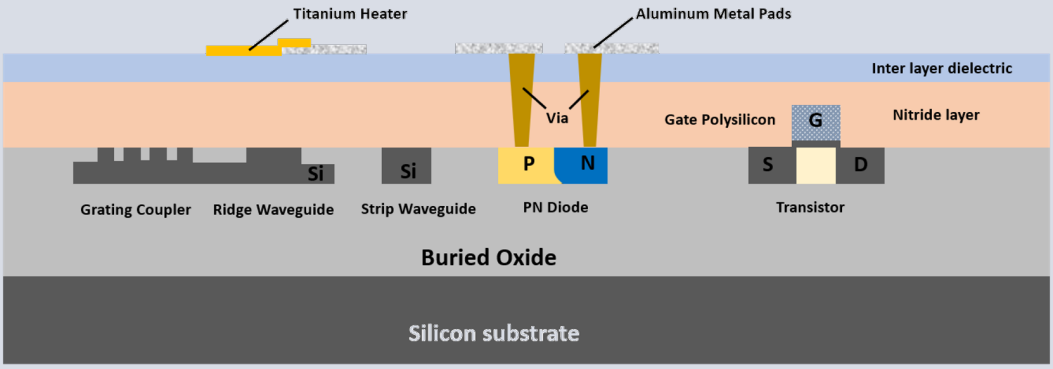


EPDA Environment



Co-simulation of electronic and photonic devices in cadence photonics tool. The electronic circuit (at the bottom) drives the photonic circuit (at the top).

Here, at IITM, we focus on co-design, co-packaging and co-integration of electronics for photonics applications. Our co-design efforts involve developing electronic driver circuits using TSMC 65nm and 28nm technologies, with a recent partnership with GlobalFoundries for 45nm SPCLO PDK for monolithic integration. In co-packaging, we collaborate with izmo Microsystems and have developed in-house photonic packaging capabilities. We are designing a CMOS driver circuit based on a Chain of Inverters (Super Buffer) and Power Amplifier using 65nm TSMC technology, optimized for high-speed, low-power operation at 1 GHz to support large-scale PPICs. Additionally, we are developing a CMOS multiplexer circuit based on zero-change Silicon Photonics technology to drive thermal tuners in PPICs.



SOI CMOS process cross-section with both electronics and photonics component

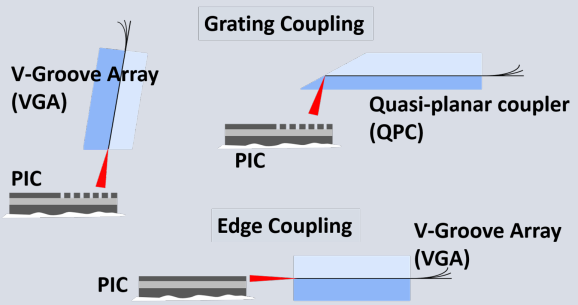
Fiber-to-Chip Attachment and Packaging with Module Development

Associated Research Scholars: *Nagarajan Nallusamy, Ankan Gayen, Shamsul Hassan, Vinoth Subramanian*

Integrated photonic components, commonly known as PICs, are manufactured using conventional semiconductor fabrication technologies and are hence highly cost effective at high manufacturing volumes with extremely small form factors. Even though such ground breaking benefits of PICs exist, their commercialization and widespread use have a major bottleneck: packaging & interfacing. Today, 70-80% of the cost of a photonic integrated module comes from the packaging and assembly process. This high cost comes due to the sophisticated manufacturing techniques that are needed to: Optically interface to the PIC, thermally manage the PIC to ensure strict temperature control and the large variety of packaging technologies that are to be simultaneously used for assembly. At CoE-CPPICS, we strive to address each one of these technology challenges to enable cost effective, efficient photonic integrated modules for information technological applications in India and the world at large.

Optical Interfacing

Optical interfacing to the PIC involves coupling the light directly from an optic fiber or an array of fibers into the photonic integrated circuit on the substrate. This can be done through the use of a grating coupler with an angled fiber (or array) or an edge coupling to a polished waveguide facet with a lensed fiber (or array). The precise alignment of the optical fiber, in each case, with the optical coupling structure on the PIC to ensure maximum mode field overlap and hence coupling is quite complex, expensive & time consuming. This is due to the fact that tolerances are limited and a 6-axis (X, Y, Z, tilt, roll, yaw) alignment is needed. In fact, for a grating coupler, tolerances are around a few microns while for an edge coupler, it can be less than 1 micron for ensuring precise mode field overlap. For the first time in India, we have developed this optical coupling technology in-house with the capability to perform single fiber, V-groove array (VGA), and Quasi-planar coupling (QPC) fiber array using the same universal setup as shown in the figure.

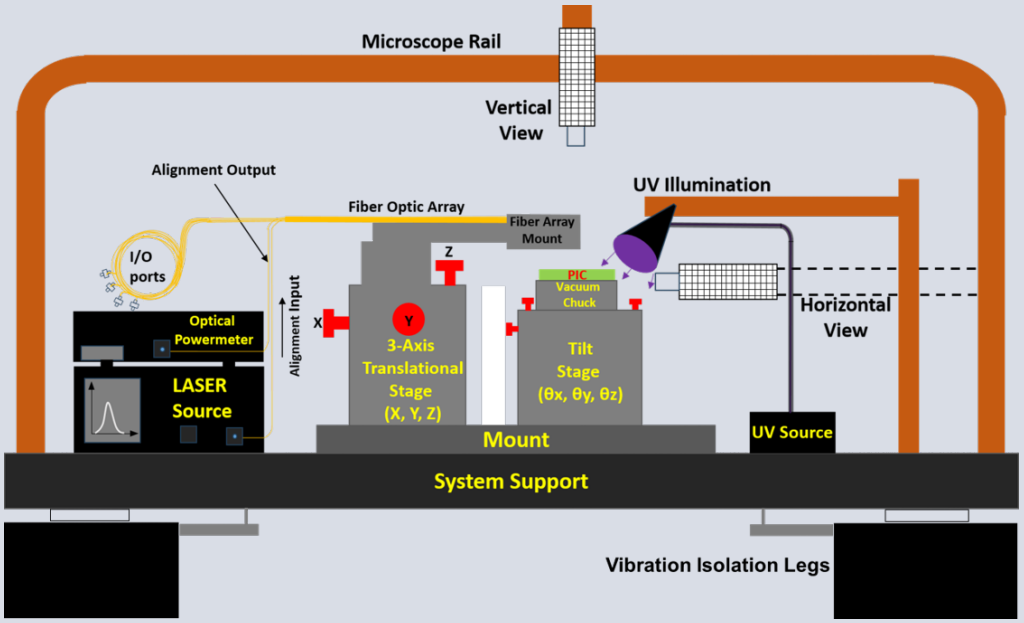


Different types of coupling schemes

Thermal Co-design

Photonic integrated circuits are highly temperature sensitive as even a slight shift in the effective refractive index of the photonic components due to a temperature change (Thermo-optic effect) can lead to a drastic change in its transmission spectrum. It is hence imperative to maintain the temperature of the PIC within fixed tolerance limits. Thermal design of the photonics module must take into account the heat generated within the PIC itself, due to on-board resistive heaters, as well as thermal crosstalk with other electronic ICs that are integrated as part of the system/module. The temperature control is hence done actively with a Thermo-Electric-Cooler (TEC) module and closed loop PID. Proper 'temperature-aware'

placement of the various components, design of the heat sink, choice of materials & full system thermal modelling is hence to be done. Such a design is possible using state-of-the-art thermal simulation tools available at CPPICS. An example case where a single fiber attachment to the PIC is successfully performed along with proper thermal design is shown in the figure. Here, optical signals can be sent into the PIC through the input fiber and the output can be taken to a photodetector through the output fiber. The mechanical strength of the fiber attachment was verified through manual shear tests.



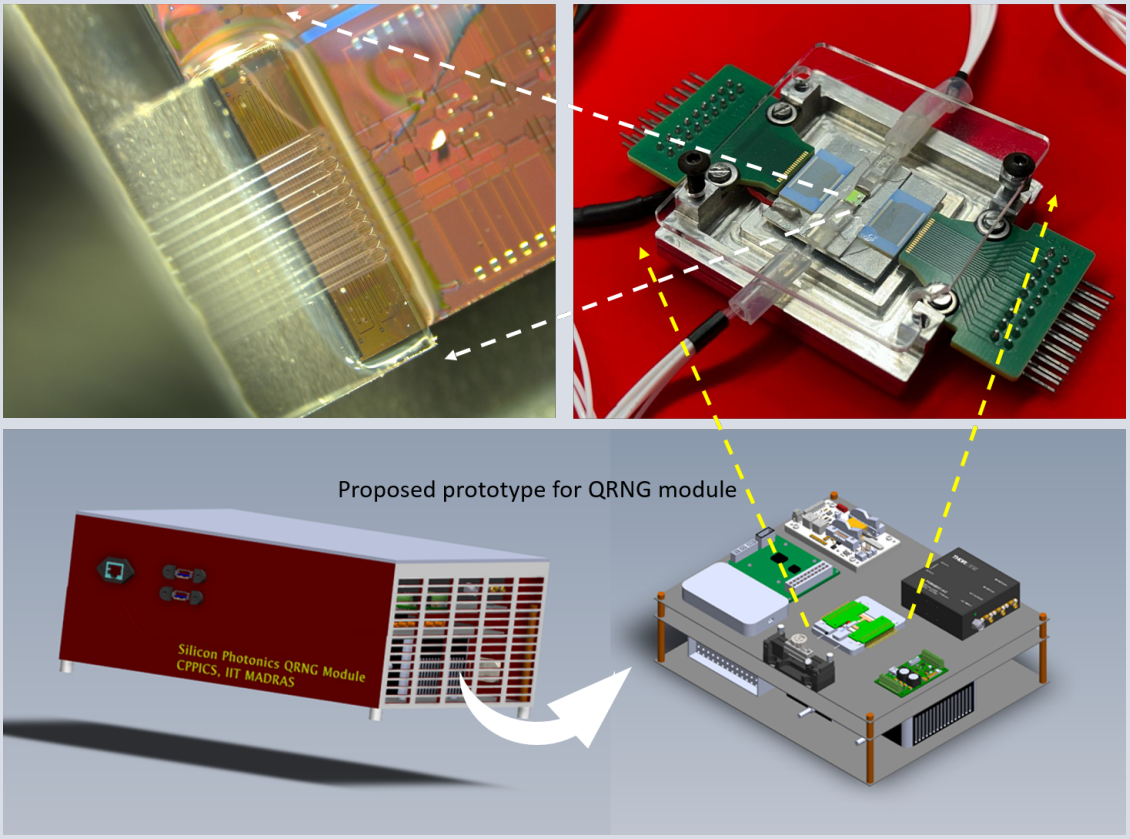
Optical coupling setup developed by CoE-CPPICS

System Integration and module development

At CPPICS, we aspire to streamline the entire photonic-integrated module design flow from the design & optimization of the PIC; optimal optical coupling to the PIC; design of electronic components on PCB; heterogeneous integration of the PIC, electronics, laser source & TEC; and the full system packaging with testing. We also work closely with out industrial partner, izmo Microsystems, Bengaluru to co-develop this infrastructure in India which will be one of a kind and serves to bring the state of the art in photonics & information technology to home turf. This will have a tremendous impact on the commercial and defense sectors. An example fully packaged demonstration of a PIC chip developed in collaboration with izmo Microsystems is shown in the figure on next page. The package consists of a PIC mounted on a heat spreader attached to a TEC. The TEC is connected to the aluminum heat spreader, as shown in the figure. The PIC is wirebonded to the PCB for external connection to the control electronics. An external PID control can be used to stabilize the temperature of the package during operation.

The figure below shows an example of a future chip-based Silicon photonics QRNG module development at CoE-CPPICS. As we can see, several components of different technologies are to be heterogeneously integrated together as part of the full system: PIC, EIC (Electronic Integrated Circuit), power modules, laser source, analog circuits like amplifiers, FPGA module, & TEC. The integration also involves the mixing and merging of different packaging & integration technologies:

6-axis alignment for optical coupling, wire bonding, solder bonding, adhesive attachment, etc. We hence find that photonic module design can be quite complex and requires the co-design of all the various components with their heterogeneous integration to meet the desired specifications. An important feature of such a heterogeneous/hybrid photonics package is the integration of all necessary optical components including an integrated laser source and photodetector as shown in the same figure.



From fiber attachment to a fully packaged chip, followed by integration with driver circuits for the QRNG module developed at CoE-CPPICS. The actual module dimensions and details of other drivers are presented in the QRNG section.

Industry Collaboration

Foundry Partner - SilTerra Malaysia Sdn. Bhd.,

The Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) at Indian Institute of Technology Madras (IIT Madras) is partnering with SilTerra Malaysia Sdn. Bhd. for Joint development of programmable silicon photonic processor chips, especially for quantum computing and communication system level applications. The other key aspects of the partnership will be joint R&D on novel silicon photonic devices and circuits for energy efficient high-speed interconnect solutions for data centres, high-performance computing, and for AI/ML applications.

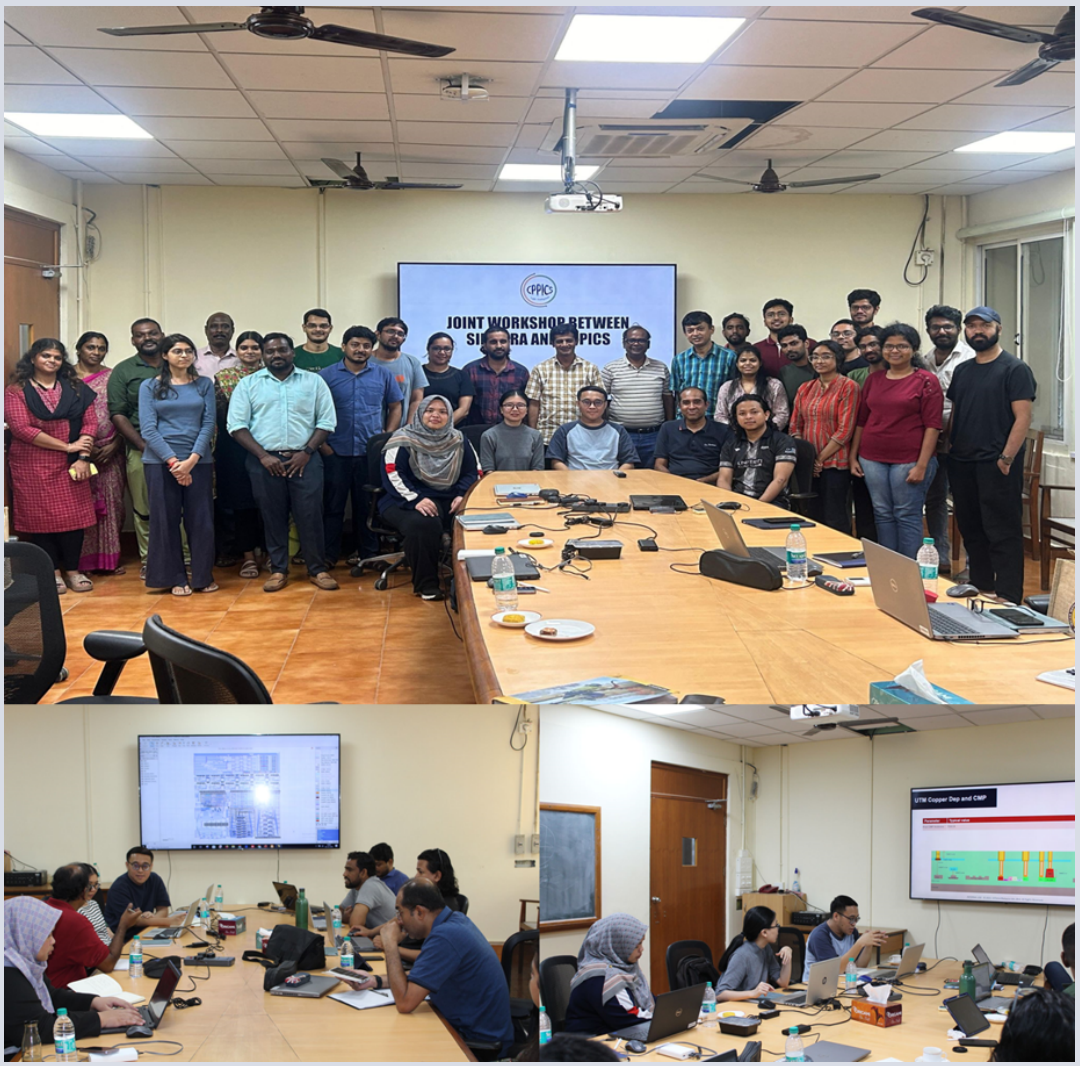
SilTerra Malaysia Sdn. Bhd., a global semiconductor foundry has been continuously innovating to bring leading-edge semiconductor solutions to transform the world through its disruptive silicon photonics process technologies. The Silicon Photonics CoE-CPPICS team at IIT Madras, India, is committed with its resources to enrich Silicon Photonics PDK libraries for SilTerra Silicon Photonics Foundry for mutual benefits.

An MoU towards this collaboration has been signed recently by Prof. Manu Santhanam, Dean (Industrial Consultancy and Sponsored Research), IIT Madras and Dr. Albert Pang Shu Koon, CEO at SilTerra Malaysia Sdn. Bhd. Other signatories include Prof. Bijoy Krishna Das, Chief Investigator of Silicon Photonics CoE-CPPICS and Mr. Thung Beng Joo, Vice President of Emerging Technologies Department, SilTerra Malaysia Sdn. Bhd.

IIT Madras Silicon Photonics CoE-CPPICS partners with SilTerra Malaysia for Joint development of programmable silicon photonic processor chips

Very recently, a productive 12-day brainstorming workshop focused on advancing silicon photonics,

with active participation from process and design engineers (Yih Loong Gan, SHI YUAN KHOR, Yusman Mohd Yusof, Intan Murni, Muhammad syamil) from our foundry partner, SilTerra Malaysia Sdn. Bhd., alongside research scholars, project engineers, post doctoral fellows (Dr. Shamsul Hassan, Dr. NAGARAJAN Nallusamy), CTO (Dr. Arnab Goswami) and faculty members (Prof. Bijoy Krishna Das, Prof. Deleep Nair, Prof. Anjan Chakravorty) associated with the Silicon Photonics CoE-CPPICS. The theme of the workshop was an in-depth review of our ongoing research outcomes and action items for upcoming fabrication tapeout and evaluation strategies. The workshop was concluded by developing a working roadmap for our ambitious objective of wafer-scale manufacturing of Silicon Photonics Enabled Quantum Circuits and Systems.

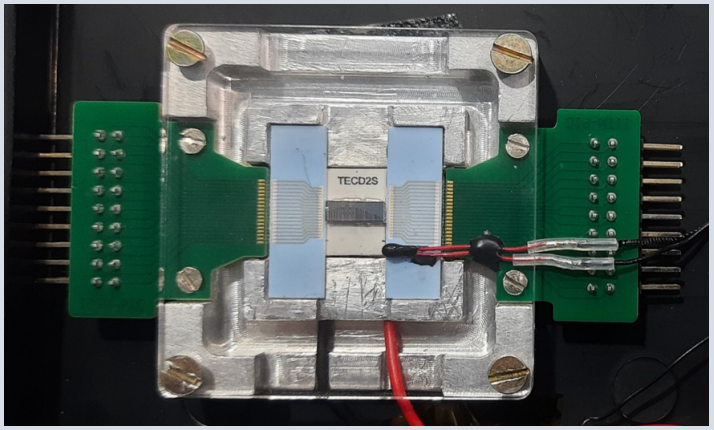


17th - 29th October, 2024: Workshop on advancing silicon photonics with SilTerra Malaysia Sdn. Bhd .

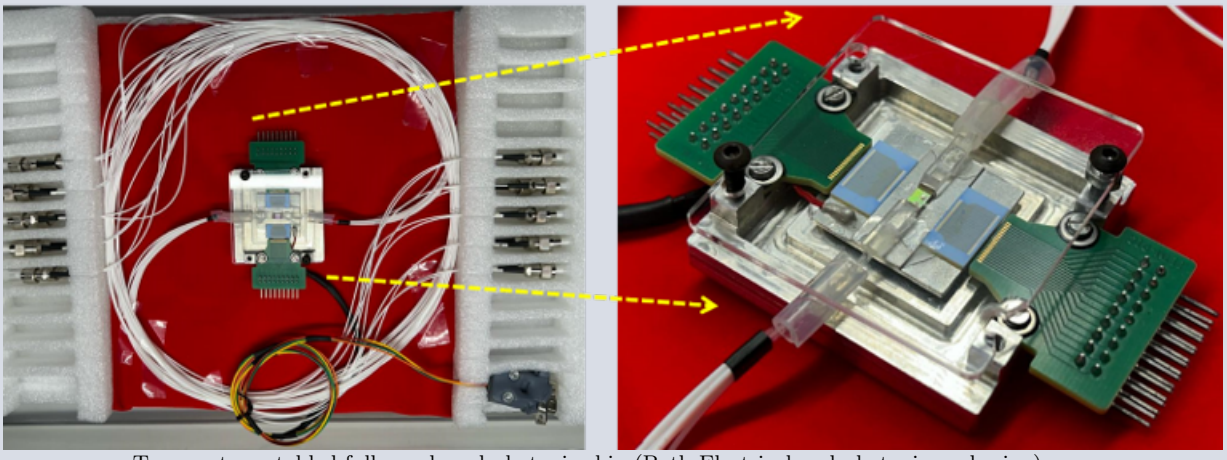
System in Package Partner - izmo Microsystems, Bengaluru, India

izmo Microsystems is the hi-tech semiconductor and systems company specializing in miniaturization using System-in-Package, with India based facilities for 3D packaging. To get a clear perspective about industry demands and to keep up with the needs of the Silicon Photonics market, we have collaborated with izmo microsystems to bring system-in-package solutions for photonic integrated circuits.

izmo Microsystems contributed 325 Lakhs to developing the fiber optic array attachment and RF PCB fabrication for silicon photonics packaging. Based on the Packaging design and simulation: (i) material selection, (ii) mechanical design, (iii) thermal and thermo-mechanic management, (iv) thermo-mechanical simulation and optimization, (v) optimization DC behavioral characteristic izmo Microsystems has developed electronic packages. These packages were designed following the silicon photonic chip design rules established by the foundry and the in-house chip development guidelines from CoE-CPPICS. In addition, the dedicated optical fiber array attachment setup is installed in the izmo Microsystems for the complete silicon photonics chip packaging, and CoE-CPPICS successfully transferred this fiber optic attachment technology to izmo microsystems, Bengaluru, India.



Prototype of electrically packaged silicon photonics chip


Temperature stabled fully packaged photonic chip (Both Electrical and photonic packaging)

EPDA Partner - Keysight Technologies, Inc. USA

The Center of Excellence for Silicon Photonics (CoE-CPPICS) at the Indian Institute of Technology Madras has partnered with Keysight Technologies to advance the compact modeling of silicon photonics components for Electronics and Photonics Design Automation (EPDA).

The collaboration is spearheaded by Mr. Mohit Khanna (R&D Manager - EDA SW Engineering) and Mr. Soumya Dey (Senior R&D Manager) from Keysight Technologies, along with Prof. Bijoy Krishna Das, Prof. Anjan Chakravorty, Prof. Deleep Nair, and CTO Dr. Arnab Goswami from IIT Madras. The team is further supported by members Mr. Ashitosh Velamuri, Ms. Suvarna Parvathy, Mr. Pawan Kumar, Ms. Shruti Pandey, and Ms. Anjana James.

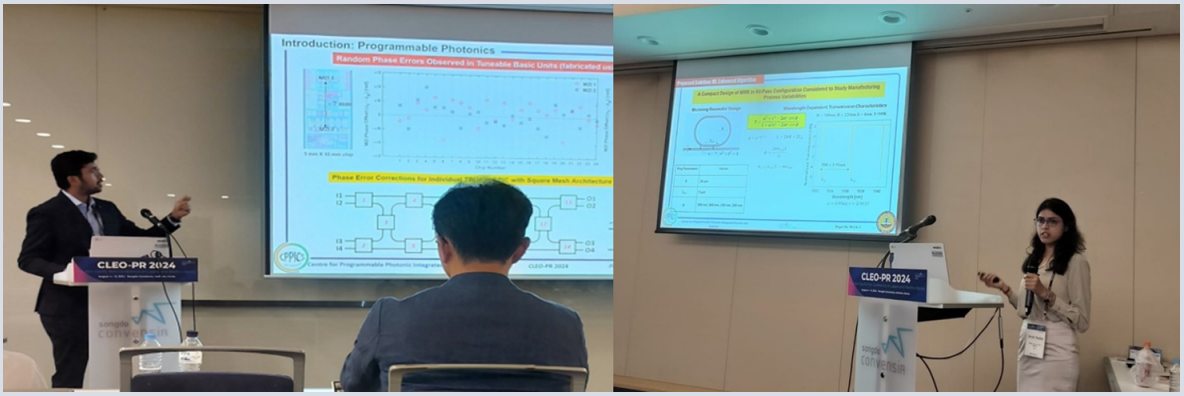
In its first phase, the project successfully implemented compact modeling of photodetectors using Keysight's Advanced Design System (ADS) software tool. Simultaneously, work is underway on the compact modeling of microring resonator (MRR)-based modulators.

The inaugural kickoff review meeting for the compact modeling of silicon photonics components under the Electronics and Photonics Design Automation initiative was held at the IIT Madras Silicon Photonics CoE-CPPICS with team members from Keysight Technologies, Inc., USA.

National and International Outreach

Over the last three years, the research and development activities of our center of excellence have been presented at various national and international conferences, seminars, and workshops.

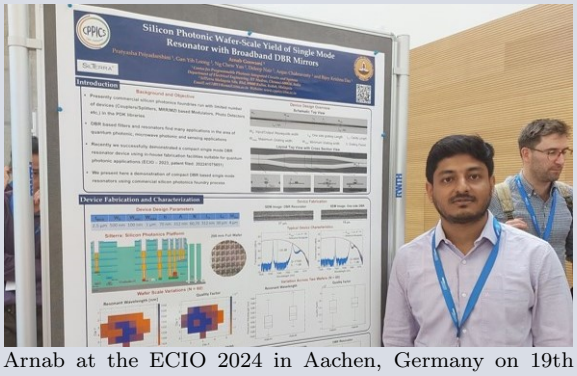
Prof. Bijoy Krishna Das visited the Institute of Photonics at Leibniz Universität Hannover, Germany, and the University of Trento, Italy, in October 2024.



Kumar Piyush and Shruti Pandey presenting their work at the CLEO-PR 2024, Incheon, South Korea

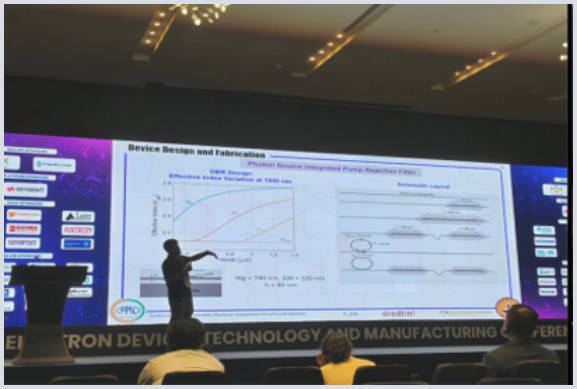
Prof. Bijoy Krishna Das presented an overview of the progress at the Silicon Photonics CoE-CPPICS at EU-India Joint Researchers Workshop on Semiconductors on October 9th in Brussels, hosted by ICOS

Anushka, Pranita, and Arnab presented their posters at the IEEE Silicon Photonics Conference 2024, held on April 18, 2024, in Tokyo, Japan.

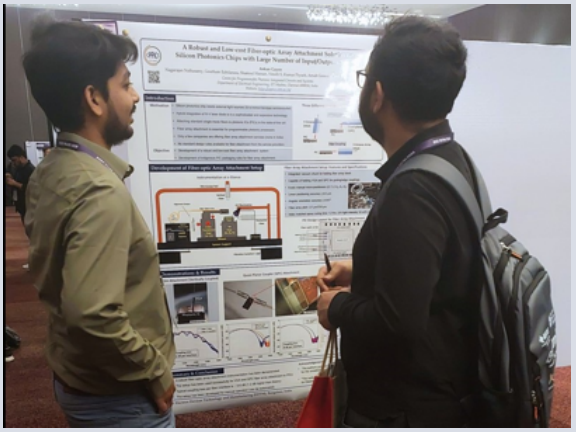


Arnab at the ECIO 2024 in Aachen, Germany on 19th June 2024

Ashitosh at OFC 2024 in San Diego, California, USA on 28th March 2024



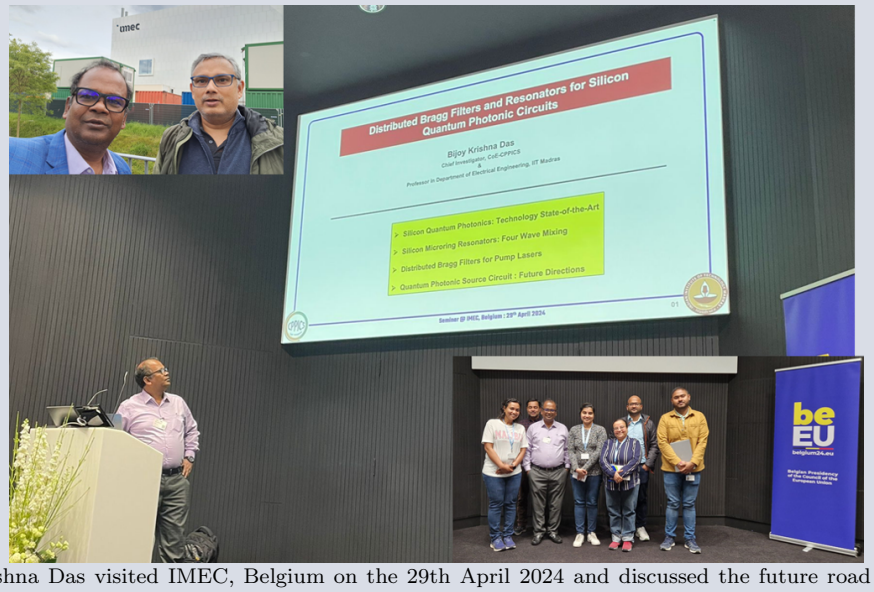
Arnab at IEEE Electron Devices Technology and Manufacturing Conference 2024 in Bengaluru, India



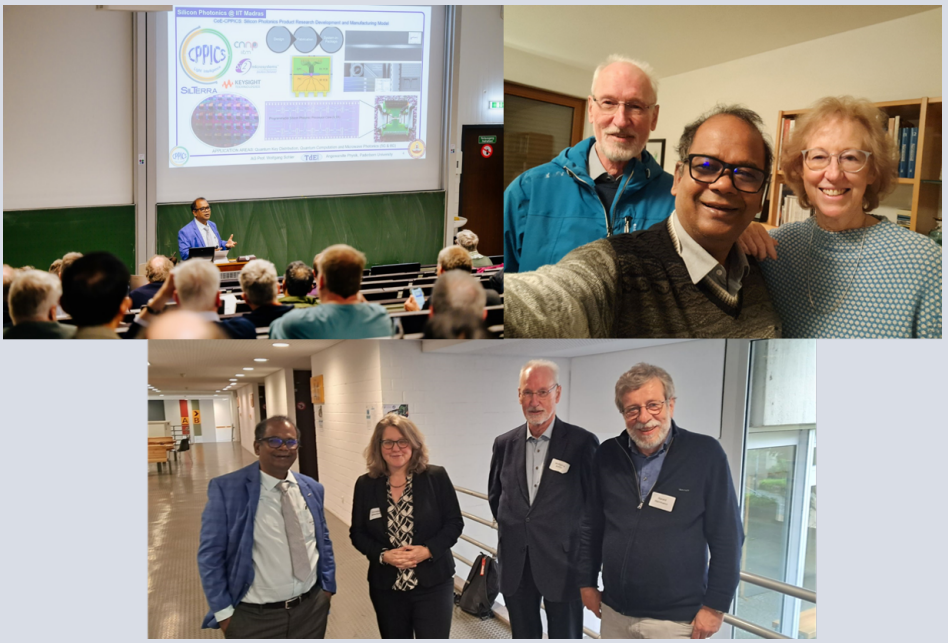
Ankan at IEEE Electron Devices Technology and Manufacturing Conference 2024 in Bengaluru , India

Our CTO, Arnab Goswami, had the opportunity to showcase our activities in quantum key distribution and quantum random number generation to Prof. Ajay Kumar Sood, Principal Scientific Adviser to the Government of India at Society for Electronic Transactions and Security (SETS), Chennai.

16th-18th May 2024: CoE-CPPICS organized an internal workshop on Silicon Photonics Enabled Quantum Photonics Circuits and Systems with SETS and IMSc, Chennai, India



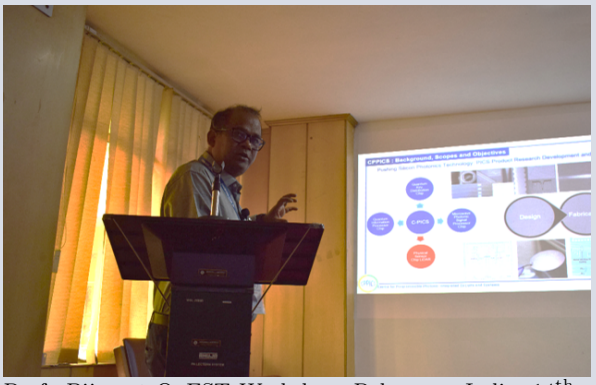
prof Bijoy Krishna Das visited IMEC, Belgium on the 29th April 2024 and discussed the future road map of silicon photonic research with Dimitrios Velenis, Sumi RadhaKrishnan.



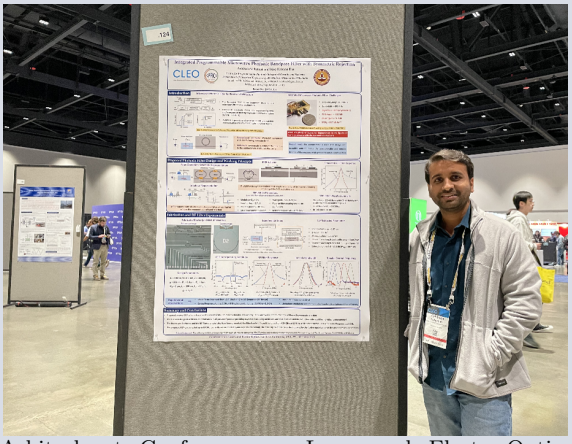
In April 2024, Prof. Das visited Paderborn University, where he had earned his Ph.D. under the guidance of Prof. Wolfgang Sohler, as part of a reunion organized by his colleagues in Germany. During the visit, Prof. Das also spent a few weeks as a guest scientist in Prof. Silberhorn's group.

13th March 2024: Visit of Dr. Sandip Chatterjee (Sr. Director, Ministry of Electronics and Information Technology, Govt of India) at CoE-CPPICS

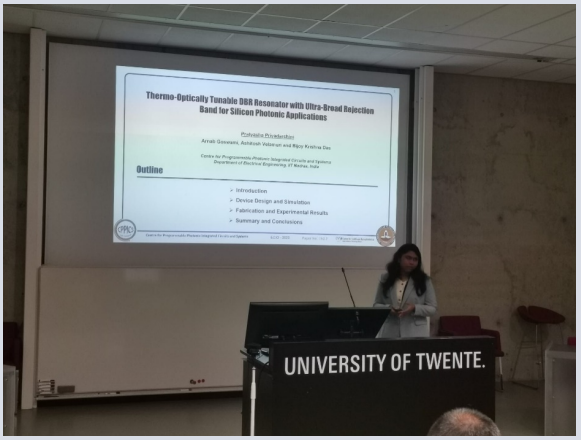
Anushka at 6th International Conference on Emerging Electronics (ICEE), Bangalore, India; 13th December 2022



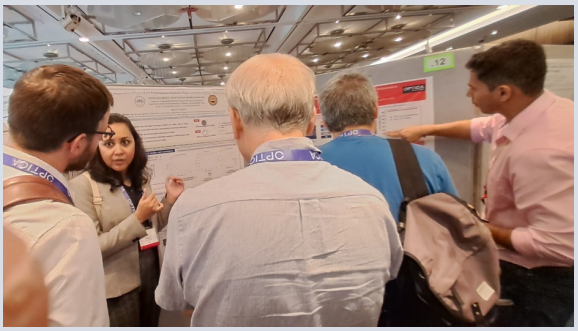
Prof. Bijoy at QuEST Workshop, Palampur, India; 14th May, 2023



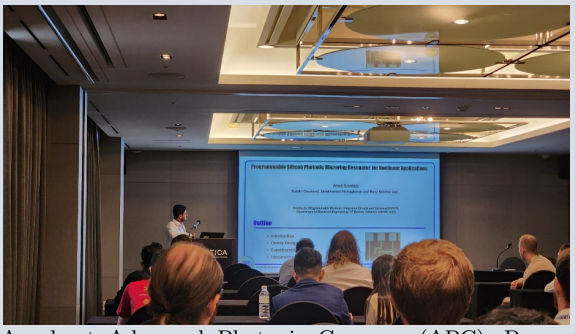
Ashitosh at Conference on Laser and Electro-Optics (CLEO), San Jose, California; 10th May, 2023



Pratyasha at European Conference on Integrated Optics (ECIO), Twente, Netherlands; 20th April, 2023



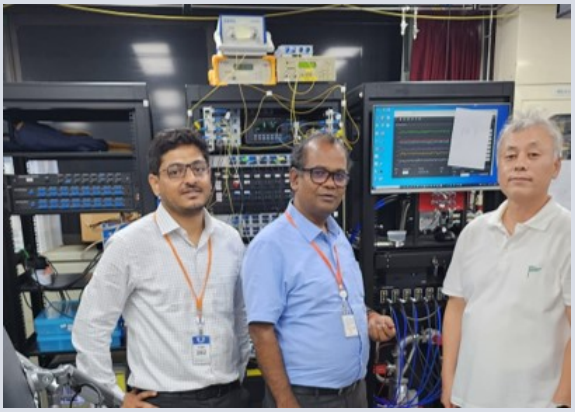
Suvarna at Advanced Photonic Congress (APC), Busan, South Korea; 11th July, 2023



Arnab at Advanced Photonic Congress (APC), Busan, South Korea; 13th July, 2023

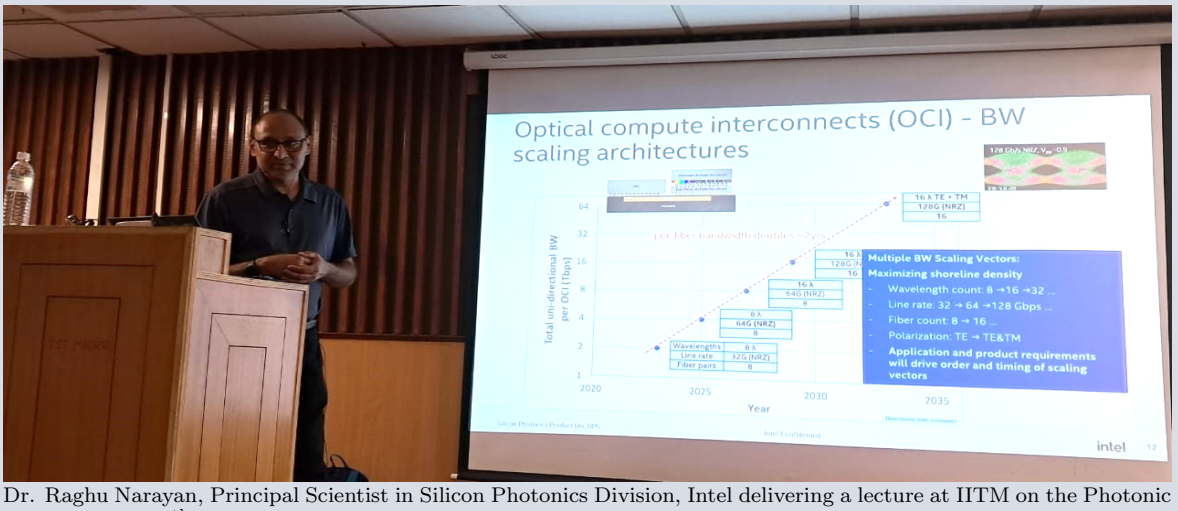
Dr. Mallik Tatipamula, CTO of Ericsson Silicon Valley during his visit to our Centre; 18th July, 2023

Mr. Kailash Narayan, President (Communications Group), Keysight Technologies at our lab; 21st April, 2023



Arnab and Prof. Bijoy at ETRI, Daejeon, South Korea with Dr, JongMoo Lee; 15th July, 2023

Conversation with Prof. Wim Bogearts at ICEE, Bangalore, India; 13th December 2022



Dr. Raghu Narayan, Principal Scientist in Silicon Photonics Division, Intel delivering a lecture at IITM on the Photonic Interconnects; 27th June, 2023

Visit of delegates (Niels Fache, Soumya Dey and Mohit Khanna) from Keysight at IIT Madras; 24th June, 2023

Our research scholars at the Workshop on Advances in Optical Communications organized at IITM Research Park; 23rd July, 2022

Our presence at Semicon India, Gandhinagar; 28th July, 2023

Lab outing with Industry Advisory Board Chairperson Dr.Mallik Tatipamula; 17th July, 2023

Ashitosh, Arnab, Dr. Sankha Dip Das and Prof. Bijoy at Digital India, Gandhinagar; 6th July, 2022

Prof. Bijoy and Arnab interacting with MeitY delegates (Dr. Sandip Chatterjee (Senior Director,MeitY), Smt. Sunita Verma (R & D Coordinator, MeitY) and Shri Alkesh Kumar Sharma (Ex. Secretary, MeitY)); 6th July, 2022

Smt. Sunita Verma (R & D Coordinator, MeitY) visiting our research facility; 20th October, 2022

Presenting Silterra 8 inch wafer to the honorable Union Minister of State for Communications, Shri Devusinh Chauhan at Workshop on Advances in Optical Communications, IITM Research Park; 23rd July, 2023

Publications

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- **These chips will be utilized for quantum computing and high-speed secured communication systems**
- **Ms. Chew Yan Ng, Deputy Director, SilTerra and Mr. Arnab Goswami, CTO at CoE-CPPICS, IIT Madras have been engaged to coordinate from both sides for technology innovations**

The Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) atIndian Institute of Technology Madras(IIT Madras) is partnering withSilTerraMalaysia Sdn. Bhd. for Joint development of programmable silicon photonic processor chips, especially for quantum computing and communication system level applications.

Theother key aspects of the partnership will be joint R&D on novel silicon photonic devices and circuits for energy efficient high-speed interconnect solutions for data centres, high-performance computing, and for AI/ML applications.

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IIT-M's CPPICS Partners with SilTerra Malaysia for Production of Silicon Photonic Processor Chips

The Silicon Photonics Centre of Excellence at IIT Madras is partnering with SilTerra Malaysia Sdn Bhd for jointly manufacturing silicon photonic processor chips, especially for quantum computing and communication system level applications.

IIT-M's CPPICS Partners with SilTerra Malaysia (Photo: ETV Bharat)

By ETV Bharat English Team
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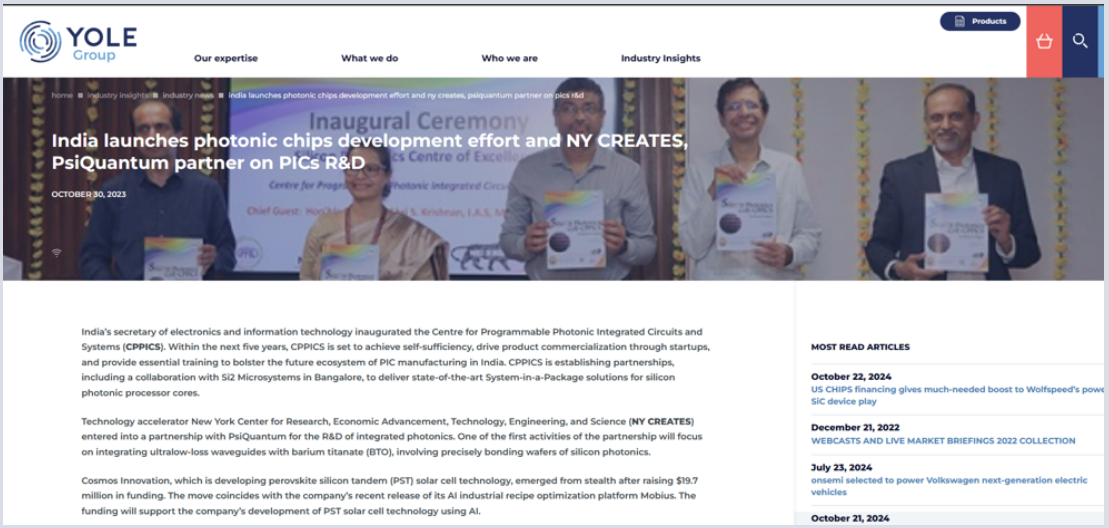
Chennai: In a noble initiative to boost quantum computing and high-speed secured communication systems in the country, the Indian Institute of Technology Madras's (IIT Madras) Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) has joined hands with SilTerra Malaysia Sdn Bhd to manufacture silicon photonic processor chips, especially for quantum computing and communication system level applications.



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India launches photonic chips development effort and NY CREATES, PsiQuantum partner on PICs R&D

OCTOBER 30, 2023

India's secretary of electronics and information technology inaugurated the Centre for Programmable Photonic Integrated Circuits and Systems (**CPPICS**). Within the next five years, CPPICS is set to achieve self-sufficiency, drive product commercialization through startups, and provide essential training to bolster the future ecosystem of PIC manufacturing in India. CPPICS is establishing partnerships, including a collaboration with Si2 Microsystems in Bangalore, to deliver state-of-the-art System-in-a-Package solutions for silicon photonic processor cores.

Technology accelerator New York Center for Research, Economic Advancement, Technology, Engineering, and Science (**NY CREATES**) entered into a partnership with PsiQuantum for the R&D of integrated photonics. One of the first activities of the partnership will focus on integrating ultralow-loss waveguides with barium titanate (BTO), involving precisely bonding wafers of silicon photonics.

Cosmos Innovation, which is developing perovskite silicon tandem (PST) solar cell technology, emerged from stealth after raising $19.7 million in funding. The move coincides with the company's recent release of its AI industrial recipe optimization platform Mobius. The funding will support the company's development of PST solar cell technology using AI.

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From left: Nagendra Krishnapura, Sunita Verma, Shri Krishnan, V. Kamakoti, and Kishore Kamath. Krishnapura and Kamakoti are members of faculty at the Indian Institute of Technology, Madras. Verma is the group coordinator for the MeitY, and Kamath is the vice president of R&D for Intel's Silicon Photonics Product Division in the U.S. Courtesy of the Indian Press Information Bureau.

ALBANY, N.Y. —Technology accelerator **New York Center for Research, Economic Advancement, Technology, Engineering, and Science (NY CREATES)** entered into a partnership with PsiQuantum for the R&D of integrated photonics. One of the first activities of the partnership will focus on integrating ultralow-loss waveguides with barium titanate (BTO), involving precisely bonding wafers of silicon photonics.

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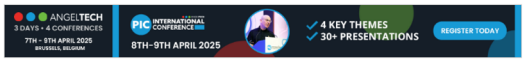

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New Delhi, Updated on Oct 20, 2023 16:28 IST

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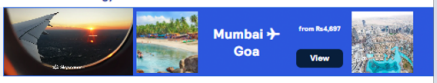

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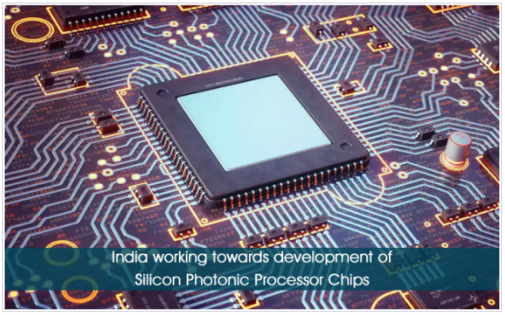

India working towards development of Silicon Photonic Processor Chips

- One remarkable achievement of MeitY's forward-thinking strategy is the establishment of the Silicon Photonics Centre of Excellence on Programmable Photonic Integrated Circuit and Systems (Silicon Photonics CoE-CPPICS) at the prestigious Indian Institute of Technology Madras (IIT Madras) under the leadership of Prof Bijoy Krishna Das, Dept. of Electrical Engineering. In December 2020, this

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MeitY, Si2 Microsystems Partner To Setup Silicon Photonics Research Centre At IIT Madras

By Yashasvini Razdan · October 31, 2023

The Indian Institute of Technology Madras (IIT Madras) has inaugurated a Silicon Photonics Research Centre of Excellence.

- *In addition to Si2, the CoE will also receive support from Intel, Keysight Technologies USA and SiTerra Malaysia.*

Ministry of Electronics and Information Technology (MeitY), along with Si2 Microsystems, has collaborated to set up a Silicon Photonics Research Centre of Excellence, Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) at the Indian Institute of Technology, Madras (IIT-M).

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IIT Madras partners with SilTerra Malaysia for silicon photonic processor chips

Updated - May 24, 2024 at 04:55 PM.

These chips will be utilised for quantum computing and high-speed secured communication systems

BY BL CHENNAI BUREAU

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A researcher at Silicon Photonics CoE-CPPICS at IIT Madras | Photo Credit:

The Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) at Indian Institute of Technology Madras (IIT Madras) is partnering with SiTerra Malaysia Sdn. Bhd. for joint development of programmable silicon photonic processor chips. This is especially for quantum computing and communication system level applications.

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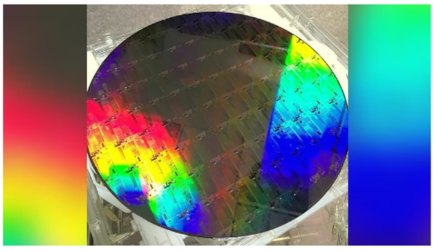
Silicon photonics for high-speed computing

Silicon photonics is the study and application of photonic systems which use silicon as an optical medium.



Silicon Photonics 300mm wafer (Photo | Wikimedia Commons)

Vaitheeswaran B

Updated on: 17 Nov 2023, 10:52 am · 4 min read

CHENNAI: On November 12, when the rest of the country was busy celebrating the festival of lights, one professor and a bunch of PhD students of IIT Madras were toiling in the laboratory to light up a 4x4 silicon photonic processor chip.

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IIT Madras and SilTerra Malaysia team up on silicon photonics

Thursday 30th May 2024

The Silicon Photonics Centre of Excellence at the Indian Institute of Technology Madras is working with semiconductor foundry SilTerra Malaysia to enrich the latter's PDK library for the production of programmable silicon photonic processor chips

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By Asia Education Review Team , Saturday, 25 May 2024 12:43:26 PM

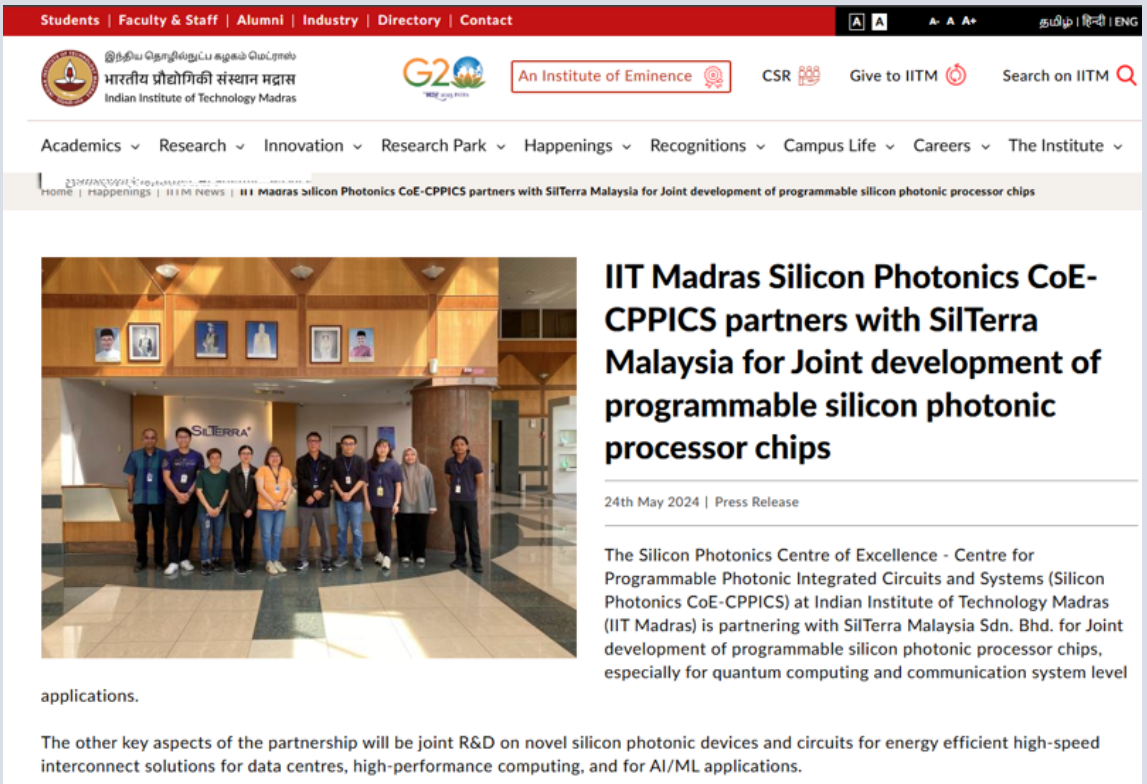
IIT Madras and SilTerra Malaysia team up for Silicon Photonic Processors

The **Silicon Photonics Centre of Excellence** - Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) at the **Indian Institute of Technology Madras** (IIT Madras) has partnered with SilTerra Malaysia Sdn. Bhd. to jointly develop programmable silicon photonic processor chips. These chips are particularly aimed at applications in quantum computing and communication systems.

The collaboration will focus on joint R&D of innovative silicon photonic devices and circuits to create energy-efficient, high-speed interconnect solutions for data centers, high-performance computing, and AI applications. SilTerra Malaysia, a leading global semiconductor foundry, will work alongside the Silicon Photonics CoE-CPPICS team, which is dedicated to enhancing the Silicon Photonics PDK libraries for the SilTerra Silicon Photonics Foundry.

V Kamakoti, Director of IIT Madras, remarked that this partnership is a significant milestone, paving the way for advancements in high-performance silicon photonics technology. As India moves toward establishing commercial semiconductor fabrication facilities, there is a growing need for research and capacity development. This collaboration aims to support that goal by advancing contemporary technologies.

Bijoy Krishna Das, Chief Investigator of CoE-CPPICS and a faculty member in the Department of Electrical Engineering at IIT Madras, highlighted that the team will leverage SilTerra's mature silicon photonics process technology from its 200 mm foundry for their R&D initiatives. In return, CoE-CPPICS will share



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IIT Madras Silicon Photonics CoE-CPPICS partners with SilTerra Malaysia for Joint development of programmable silicon photonic processor chips

24th May 2024 | Press Release

The Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits and Systems (Silicon Photonics CoE-CPPICS) at Indian Institute of Technology Madras (IIT Madras) is partnering with SilTerra Malaysia Sdn. Bhd. for Joint development of programmable silicon photonic processor chips, especially for quantum computing and communication system level applications.

The other key aspects of the partnership will be joint R&D on novel silicon photonic devices and circuits for energy efficient high-speed interconnect solutions for data centres, high-performance computing, and for AI/ML applications.

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News | May 24, 2024

IIT Madras Silicon Photonics CoE-CPPICS Partners With SilTerra Malaysia For Joint Development Of Programmable Silicon Photonic Processor Chips

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Indian Institute of Technology
Madras