Centre for Programmable Photonic Integrated Circuits and Systems

Centre of Excellence

Funded by

सत्यमेव जयते

MeitY

Government of India

IoE Research Centre, IIT Madras

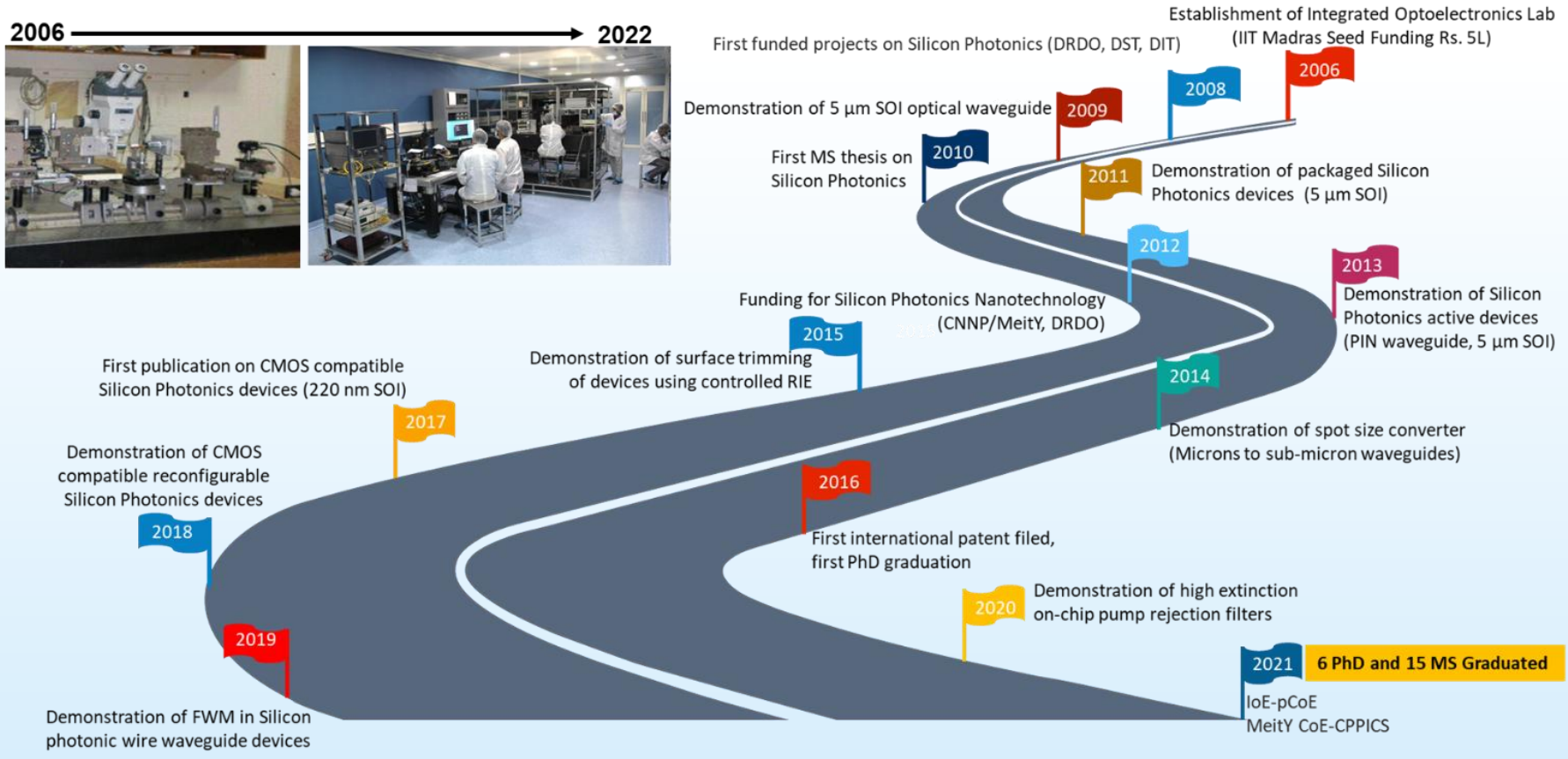
Digital India

Power To Empower

Dept. of Electrical Engineering
IIT Madras, Chennai 600036, India
www.cppics.iitm.ac.in

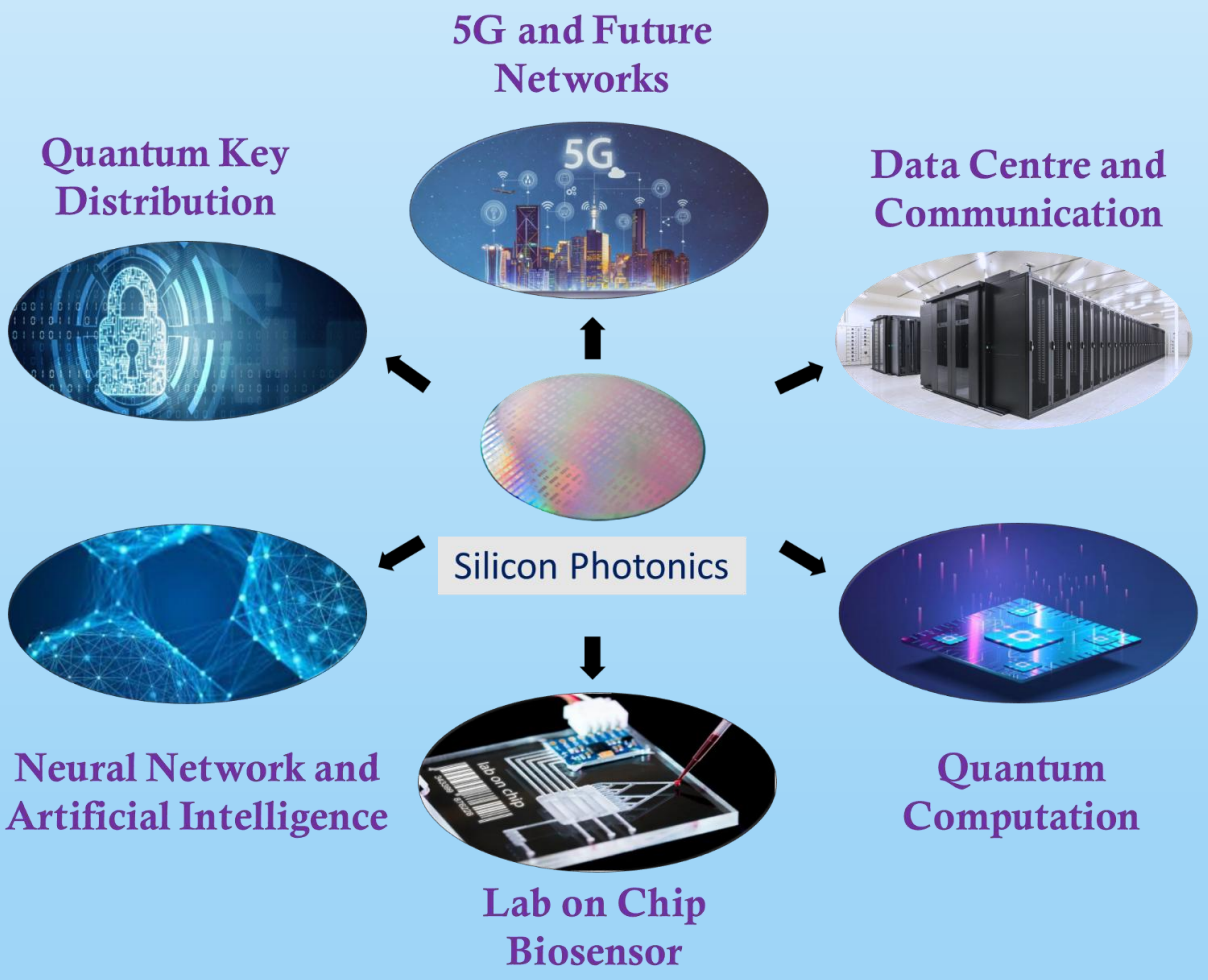
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

Our Journey since 2006



Current Research Activities

Present research focus of the CPPICS team is mainly centering around design, demonstration and packaging of photonic chips for advanced microwave and quantum photonic applications.



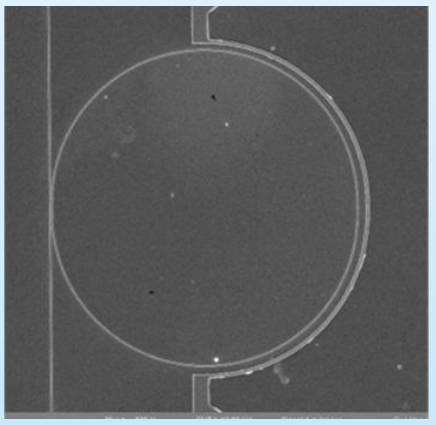
Technology Platform

CMOS compatible silicon photonics technology is our overall driving force. In general, there are two types of optical waveguide cores used for silicon photonic integrated circuits: (i) Si photonic wire waveguides in SOI and (ii) SiN waveguides on the surface of oxide grown bulk silicon substrate. We have already developed state-of-the-art SOI based silicon photonics technology over the years and very recently started working on developing SiN waveguide process technology. We are also open to access commercial silicon photonics foundries through multi-project wafer (MPW) runs.

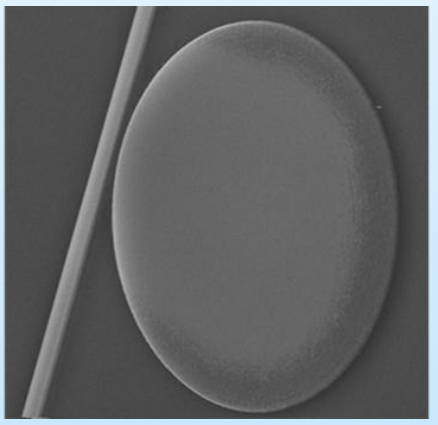
Silicon Waveguide Technology (In-house)

Some of our fabricated high performance devices are Microring Resonators (MRRs), Distributed Bragg Reflectors (DBRs) based High Extinction Pump Rejection Filters, Wavelength Independent Power Splitters, ASE Rejection Filters, MZI based Programmable Tunable Basic Units (TBUs)

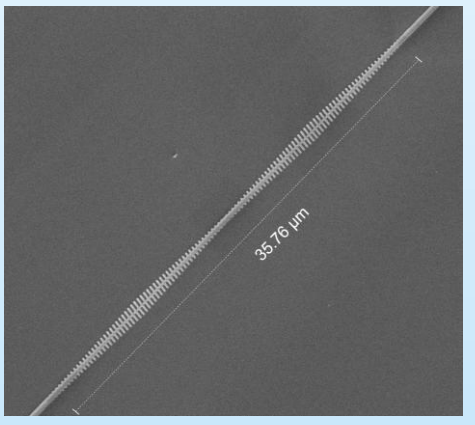
Tunable Mirroring Resonator



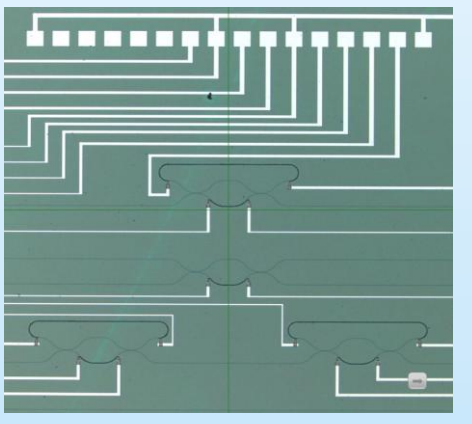
Disk Resonator



Broadband DBR stopband Filter

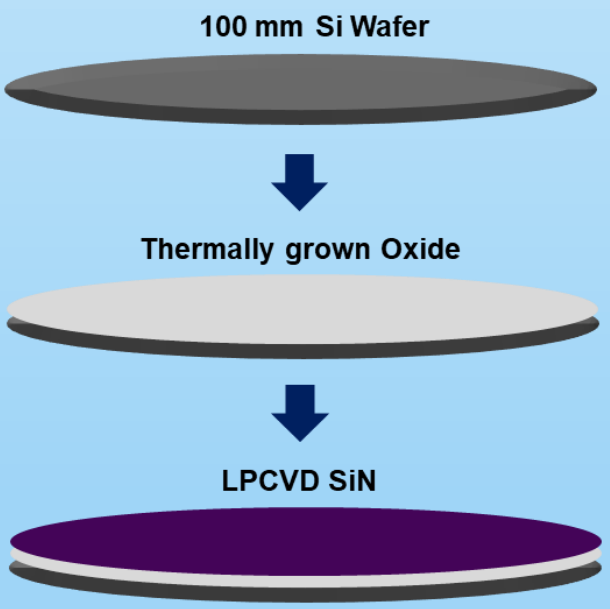


Tunable Filter for RF Photonics

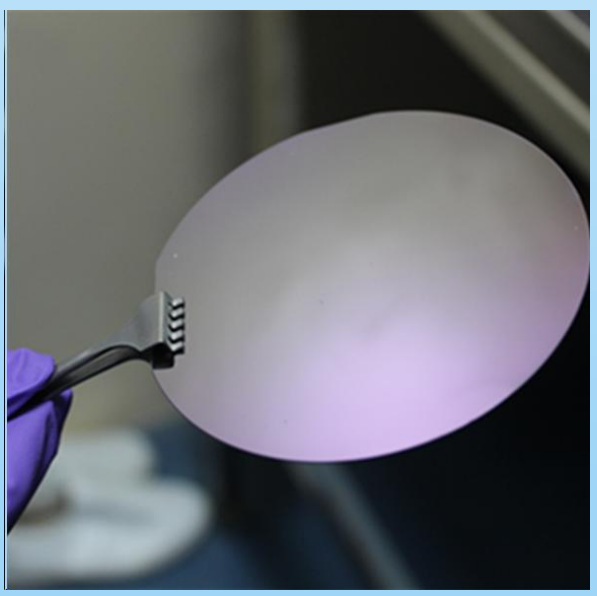


Silicon Nitride Waveguide Technology (In-house)

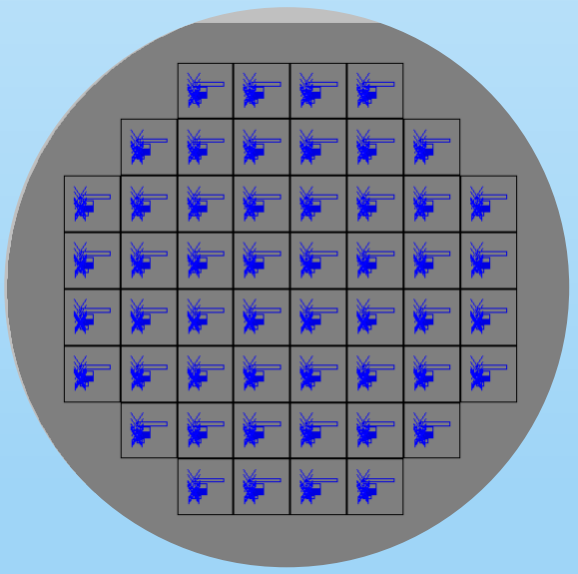
The deposition of stoichiometric silicon nitride film has been optimized using LPCVD on a 4 inch wafer with a thickness up to 400 nm with less than ±2 % variation. We aim to demonstrate low loss silicon nitride based photonic devices for different applications in Microwave and Quantum photonics.



In-house Fabricated SiN Wafer

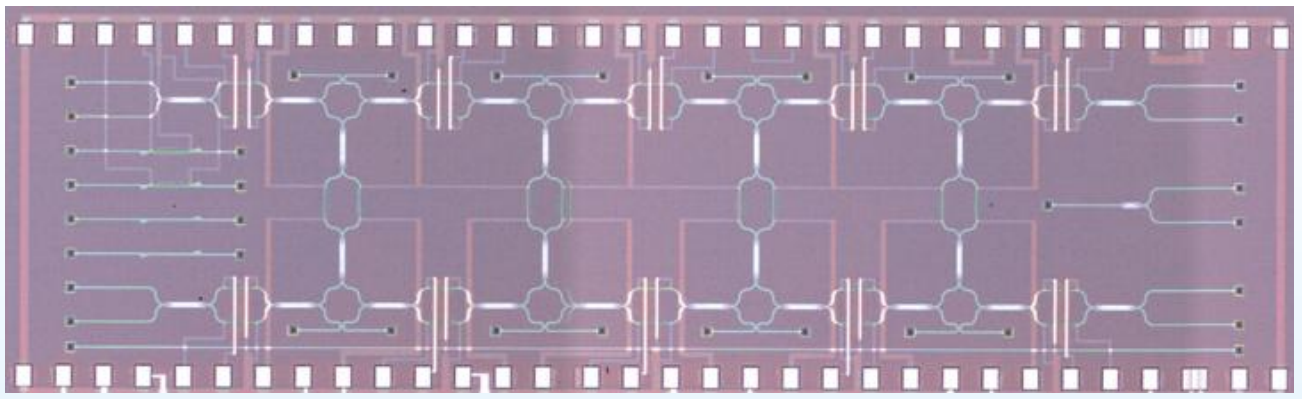


Wafer Scale Process Development

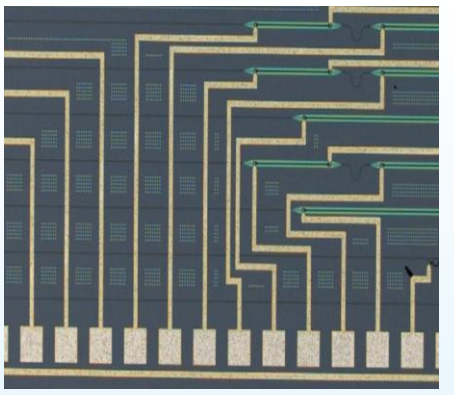


Circuit Design & Demonstration through MPW Runs

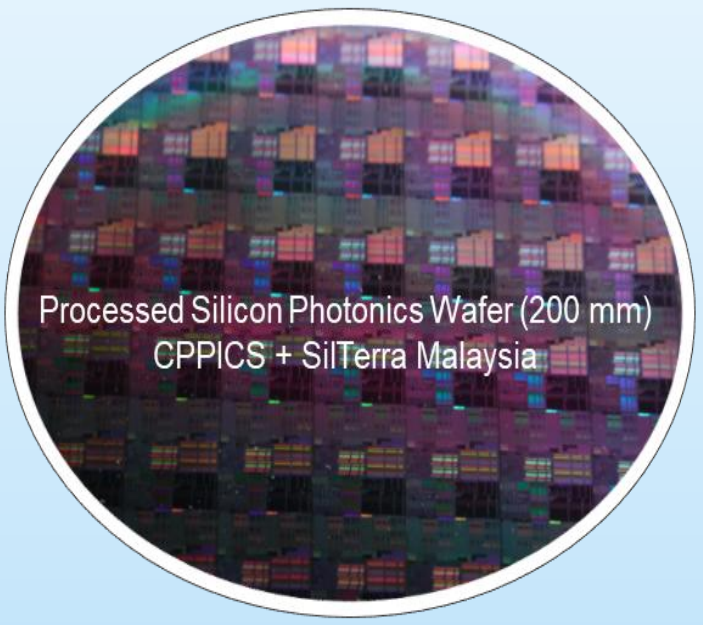
Programmable Square Mesh Architecture (IMEC, Belgium)



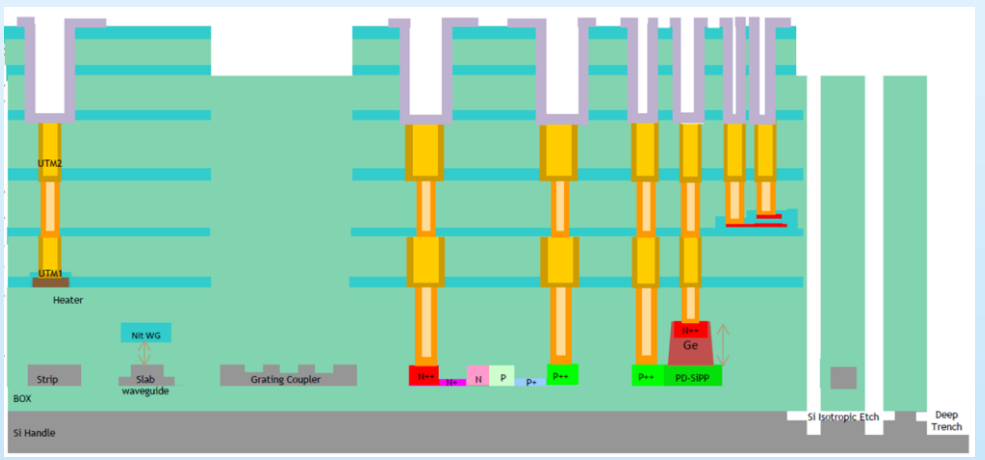
Entangled Photon Pair Generator
(AMF, Singapore)



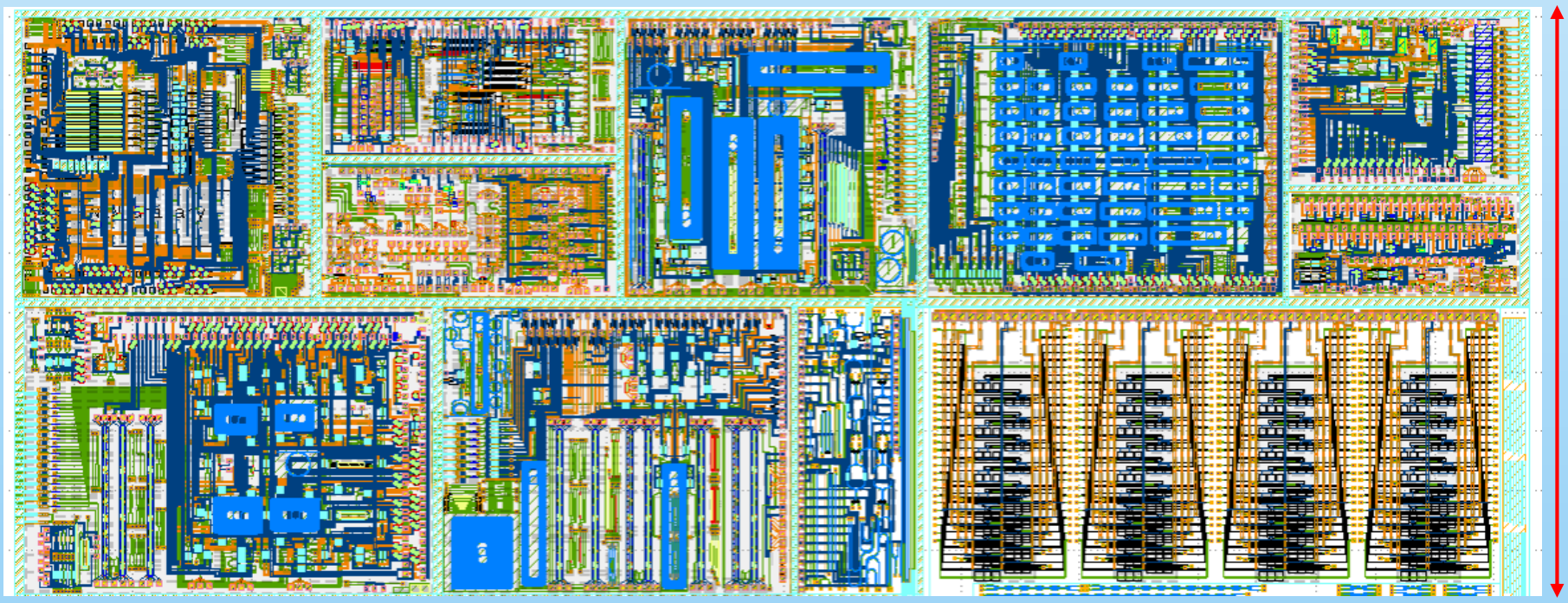
PDK Development for Silicon Photonics Technology with SilTerra, Malaysia



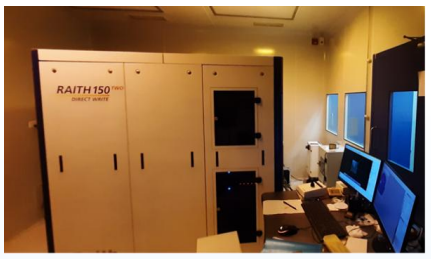
Silicon Photonics Technology Platform



Latest PIC Layout for Foundry Tapeout at SilTerra (Various Designs for Prototype Development)



Photonic Chip Design, Fabrication & Characterization:



Cleanroom facilities spreading over 5000 Sq.ft.

Major Process Tools:

- ❑ E-Beam Lithography
- ❑ DUV and i-line Lithography
- ❑ Laser Mask Writer
- ❑ ICP RIE and Deep RIE
- ❑ Metallization and Sputtering
- ❑ LPCVD and PECVD
- ❑ Oxidation and Diffusion
- ❑ Chemical Mechanical Polishing

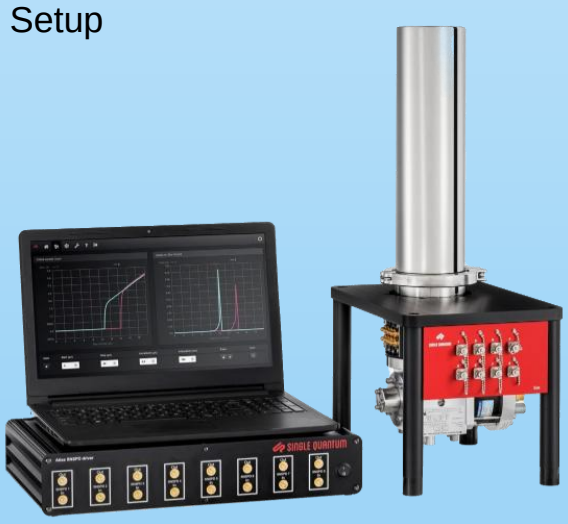
Simulation Tools:

- ❑ Ansys Lumerical
- ❑ Ansys HFSS
- ❑ Keysight ADS
- ❑ Cadence
- ❑ COMSOL Multiphysics
- ❑ Synopsys

2500 sq. ft. of Design and Characterization Labs

Major Characterization Tools:

- ❑ Wafer-scale fully automated silicon photonics probe station
- ❑ Indigenous chip-scale silicon photonics probe station
- ❑ Superconducting Nanowire Single Photon Detector Systems
- ❑ Lightwave Component Analyzer and Vector Network Analyzer
- ❑ High Resolution Optical Spectrum Analyzer
- ❑ Fiber Pigtailing and Packaging Setup
- ❑ Real-time Digital Oscilloscope
- ❑ Arbitrary Waveform Generator



Photonic Chip Assembly & Fiber Attachment:

We are in a process of developing state-of-the-art photonic chip assembly and fiber attachment facilities. Some of our commissioned facilities and indigenous setup under development have been highlighted here.

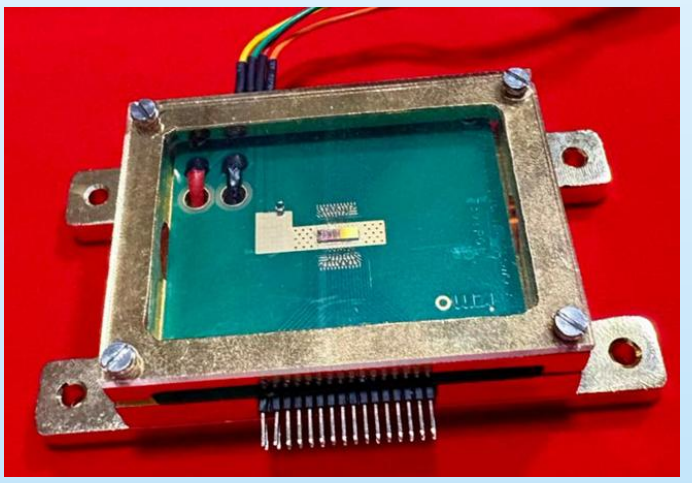
Wafer Planarization
(Upto 100 mm wafer)

Wafer Dicing Machine (upto
150 mm wafer)

Waveguide Edge Polishing System (upto
0.1 µm)

Wire Die Bonder
(Up to 25 Mil)

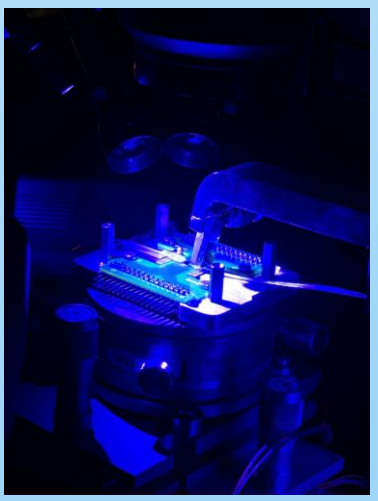
PIC Electrical Packaging

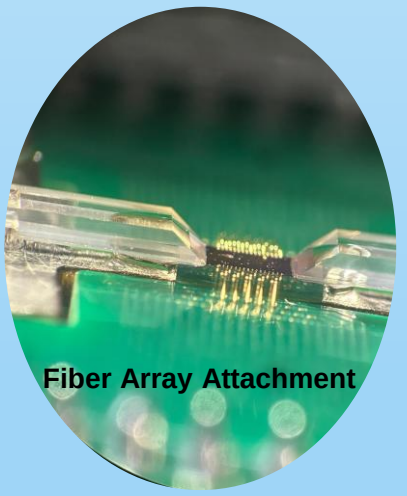


Photonic packaging and assembly is a complex and multi-disciplinary design and manufacturing process. To make a PIC-enabled module to perform according to specification, sub-micron precision alignment and bonding process are required. At the same time, precise thermal management is required to maintain the thermo-optic stability of the signals. We have collaborated ourselves with Izmo Microsystems, a company that works in the development of packaged integrated circuits, to overcome the existing limitations.

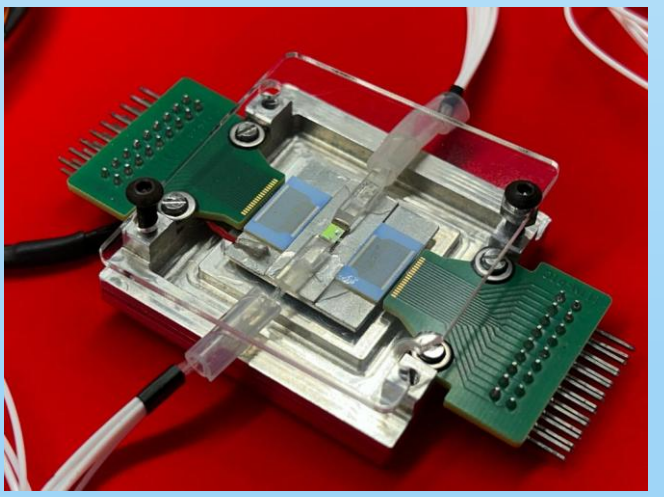
Fiber-Array Unit (FAU) Attachment Tool (Indigenously Developed)

Our indigenous setup to couple light from/to optical fiber or V-Groove Array (VGA) to/from a photonic chip, where VGA is an array of optical fibers placed together with precise spacing so that we can couple light to/from the photonic chip at multiple optical inputs/outputs simultaneously. Using this setup one can precisely place a VGA on its holder set up so that it can be aligned with the photonic chip with the sub-micron level of precision for optical i/o coupling.





Fiber Array Attachment



Chief Investigator:

Dr. Bijoy Krishna Das

Professor in Electrical Engineering

Expertise : Silicon Photonics

Chief Technology Officer:

Dr. Shamsul Hassan

Email: cto-cppics@ee.iitm.ac.in

Expertise : Silicon Photonics

Dr. Arnab Goswami

External Technology Advisor (Honorary)
Expertise : Silicon Photonics

Co-Investigators:

Dr. Amitava DasGupta

Professor in Electrical Engineering

Expertise : Device Modeling & VLSI Technology

Dr. Anil Prabhakar

Professor in Electrical Engineering

Expertise : Quantum Photonics

Dr. Anjan Chakravorty

Professor in Electrical Engineering

Expertise : Compact Modeling

Dr. Deelep R. Nair

Professor in Electrical Engineering

Expertise : Design, Fab and Testing

Dr. Deepa Venkitesh

Professor in Electrical Engineering

Expertise : Fiber Optics & RF Photonics

Dr. Enakshi Bhattacharya

Professor in Electrical Engineering

Expertise : MEMS & Photonics

Dr. Janakiraman Viraraghavan

Associate Professor in Electrical Engineering

Expertise: Circuit Design, Fab and Testing

Dr. Nandita DasGupta

Professor in Electrical Engineering

Expertise: Microelectronics & Photonics

Dr. Sargunaraj Christopher

Professor in Electrical Engineering

Expertise : Microwave Engineering

Dr. Sankaran Aniruddhan

Professor in Electrical Engineering

Expertise : RFIC Design

Industry Advisory Board :

CHAIRMAN

Dr. Mallik Tatipamula

CTO at Ericsson
San Jose, California, USA

Message from the Chairman-

I am delighted that the Centre of Programmable Photonic Integrated Circuit & Systems (CPPICS) has been engaged with cutting edge technology R&D activities under the leadership of Prof. Bijoy Krishna Das. The progress of CoE-CPPICS has been commendable during the last couple of years and its future R&D roadmap has been well planned complying with the immediate needs of silicon photonics/electronics industries. As the chairman of CPPICS Industry Advisory Board, I am committed to coordinate with other board members to provide guidance to the team CoE-CPPICS to continue its activities following the Product Research Development and Manufacturing Model.

MEMBERS

Dr. Albert Pang
CEO
SilTerra Malaysia Sdn. Bhd

Mr. Arjun Kumar Kantimahanti
R&D Engineer (Optical Systems)
Broadcom, USA

Dr. Prith Banerjee
CTO, Ansys Inc.
Palo Alto, California, USA

Dr. Vivek Raghunathan
Founder & CTO
Xscape Photonics Inc., USA

Mr. Kailash Narayanan
President and General Manager
Keysight Technologies, USA

Mr. Vijay Janapaty
Vice President and General Manager
Broadcom Inc., USA

Dr. Steve Johnston
Vice President
Merck KGaA Darmstadt, Germany

Dr. Ravi M. Bhatkal
Managing Director
India Element Solutions Inc, India

Mr. Dinanath Soni
Executive Director,
Izmo Microsystems, India

Mr. Vikas Gupta
Senior Director
GlobalFoundries USA

Mr. Narayan Srinivasa
Director
Intel Corporation USA

Dr. Kishore Kamath
Vice President and General Manager
Intel Corporation USA

Industry Collaborators:

Foundry Partner

SILTERRA, Malaysia is our Silicon Photonics foundry partner. We have been committed for a joint R&D on Silicon Photonics technology and various applications. Team CoE-CPPICS will contribute with component design, characterizations and compact modelling towards Process Design Kit block development.

Photonics Chip Packaging Partner

Izmo Microsystems, Banaglore is a hi-tech semiconductor and systems company specializing in miniaturization using System-in-Package, with India based facilities for 3D packaging. To get a clear perspective about industry demands and to keep up with the needs of the Silicon Photonics market, we have collaborated with Izmo Microsystems to bring system-in-package solutions for photonic integrated circuits.

Modeling and Testing Partner:

Keysight Technologies USA and CoE-CPPICS have signed MoU to establish an advanced silicon photonics chip testing facility at IIT Madras and exploring together on innovative solutions for electronic-photonic design automation.

Academic Collaborators :

In pursuit to maintain our high standards of research and development in the field of Silicon Photonics, we have stepped forward to link up with renowned researchers. Such collaborations come useful while exchanging ideas and knowledge with various research groups in our field. CoE-CPPICS has been immensely benefitted in its formation from the following three experts:

Dr. Natarajan Venkatachalam

Quantum Security

SETS Chennai

Dr. M PremLaxman Das

Cryptology & Computing Research

SETS Chennai

Prof. Sibasish Ghosh

Theoretical Physics

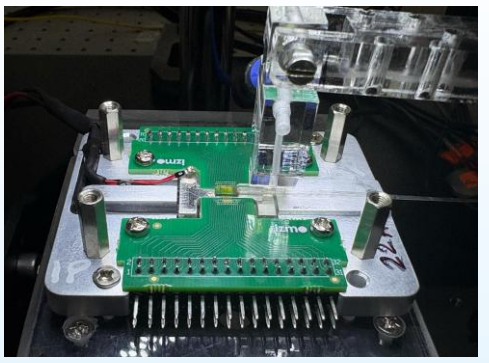
IMSc Chennai

Technology Transfer:

Fiber-optic Array Attachment for Photonic Chip Packaging

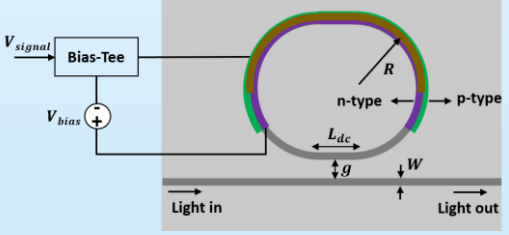
We have transferred our advanced photonic chip packaging technology to IZMO Microsystems. Building on their expertise in electronic chip packaging, IZMO is now equipped to deliver complete electrical and fiber-optic packaging solutions for photonic integrated circuits. This collaboration strengthens the ecosystem for scalable, high-performance photonic technologies.

PIC Packaging @Izmo Microsystems

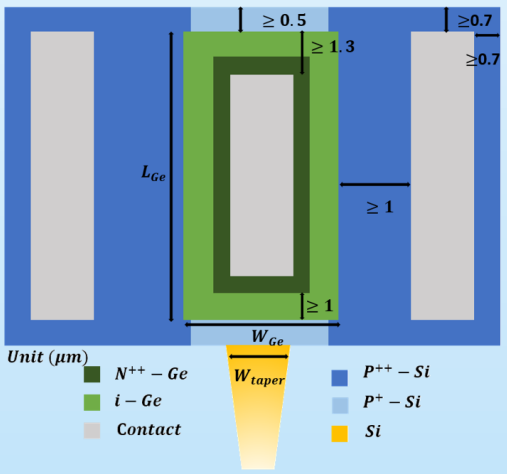


Verilog-A Models of Photonic Devices

Microring Modulator



Photodetector



We have developed Verilog-A based compact models for key photonic devices, like microring modulators and Ge photodetectors. These models have been successfully transferred to Keysight Technologies to enable seamless electronic-photonic co-design. This initiative strengthens our contributions toward accelerating design automation for integrated photonic circuits.

Quantum Random Number Generator Module

The team CoE-CPPICS has developed silicon photonics based QRNG (Quantum Random Number Generator) module and deployed at SETS (Society for Electronic Transactions and Security) Chennai for use-case applications. The 1st QRNG module is delivered to by DRDO DYSL-QT under a CARS project.

Services & Training

- ❑ Consultancy services for Photonics Chip Design and Fabrication
- ❑ Hands-on Training for Photonics Device Design and Fabrication
- ❑ Silicon Photonic Wafer-scale and Die-level Test Service
- ❑ Photonic IC Fiber Pigtailing and Packaging Services
- ❑ Workshops/Short-Term Courses on Integrated Photonics

Scan Here to Know More

Please feel free to contact us for any service related queries to : coe.service@cppics.iitm.ac.in

CPPICS Team

Feedback from our PhD Graduates

Dr. Ashitosh Velamuri

Graduation Year: 2025

Post-doctoral Researcher
Paderborn University

"The world class characterization facility at CoE-CPPICS has enabled me to perform state-of-the-art R&D in my PhD program"

Dr. Arnab Goswami

Graduation Year: 2024
Member of Technical Staff
CSpeed Inc., USA

"CPPICS offers a world-class research ecosystem, where I gained hands-on experience in device design, fabrication, characterization, and packaging"

Dr. Riddhi Nandi

Graduation Year: 2021
Principal Design Engineer
Global Foundries Pvt. Ltd, India

"The learning obtained during fabrication; characterization provides an edge over others"

Dr. Sumi Radhakrishnan

Graduation Year: 2020
R&D Engineer
IMEC Belgium

"I feel privileged to use the state-of-the-art CNNP facilities as part of my PhD program".

Dr. Ramesh Kudalippalliyalil

Graduation Year: 2019
Postdoctoral Research Associate
University of Maryland, USA

"It was amazing and unique research experience with a supporting team and well-developed infrastructure."

Dr. Parimal Sah

Graduation Year: 2018
Assistant Professor
Bhagalpur College of Engg. , India

"Working in CPPICS helped me to learn design, simulation, fabrication and characterization of integrated optoelectronic devices"

.

Dr. Sujith Chandran

Graduation Year: 2017
Research Engineer (ISI)
University of Southern California, USA

"I feel honored to be the part of CPPICS, great work culture and an Ideal group to learn from the fundamentals"

Dr. Shantanu Pal

Graduation Year: 2016
Principal Design Engineer
Global Foundries Pvt. Ltd, India

"It was a great experience in CPPICS – learned how to do research starting from building experimental lab to publish papers in international journals."