Centre for Programmable Photonic Integrated Circuits and Systems

Centre of Excellence

Funded by

सत्यमेव जयते

MeitY

Government of India

IoE Research Centre, IIT Madras

Digital India

Power To Empower

Dept. of Electrical Engineering
IIT Madras, Chennai 600036, India
www.cppics.iitm.ac.in

INDIAN INSTITUTE OF TECHNOLOGY MADRAS

Centre for Programmable Photonic Integrated Circuits and Systems

Dept. of Electrical Engineering
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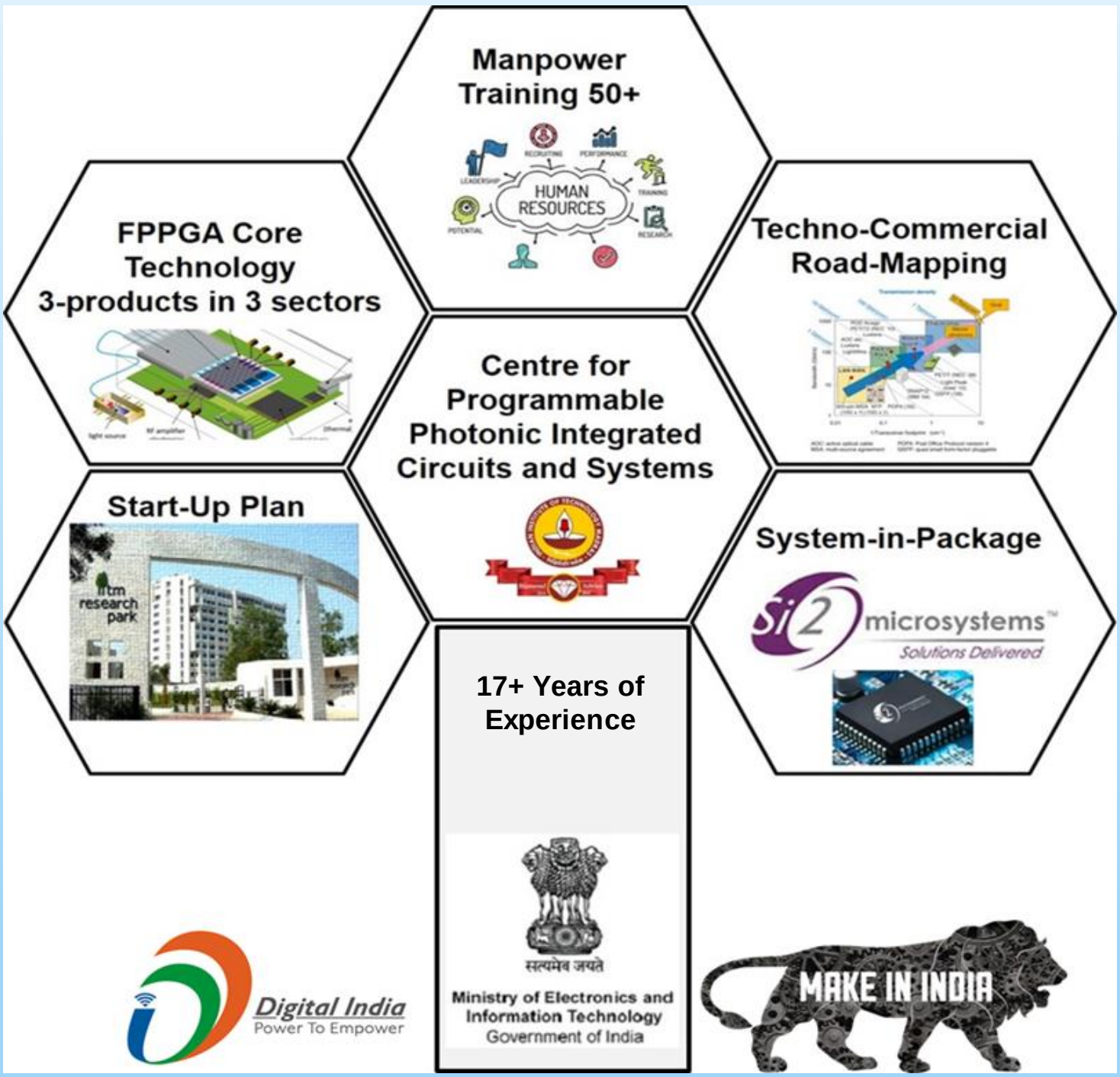
Mission Statement

Our mission is to build capacity in all verticals of silicon photonic integrated circuits manufacturing eco-system through focused R&D and nurture Indian photonics industry for immediate needs in domestic and international markets.

Background and Funding Status

The CoE-CPPICS has been established on 1st January 2021 in the Department of Electrical Engineering, IIT Madras with a substantial seed funding of Rs. 2,665 Lakhs (USD 3.5M) from the MeitY, Govt. of India, (Sanction No. GG-11/15/2020/EMCD, dated 29.12.2021), in-kind contribution of Rs. 325 Lakhs (USD 0.5M) from the Si2 Microsystems Bangalore and subsequent additional funding of Rs 425 Lakhs (USD 0.7M) from IIT Madras. This recognition and funding has been possible because of 14 years (since 2006) of R&D work by the Integrated Optoelectronic Research Group led by Prof. Bijoy Krishna Das in the area of silicon photonics technology.



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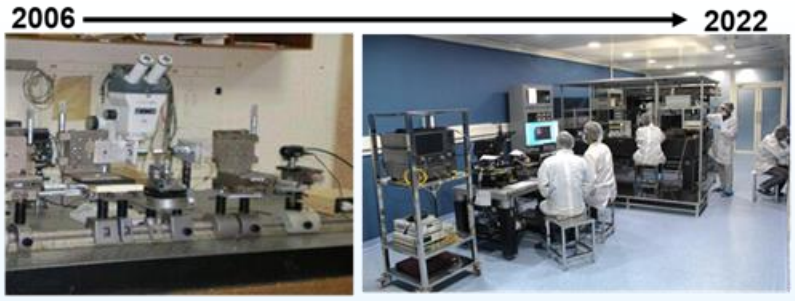
Our Journey since 2006



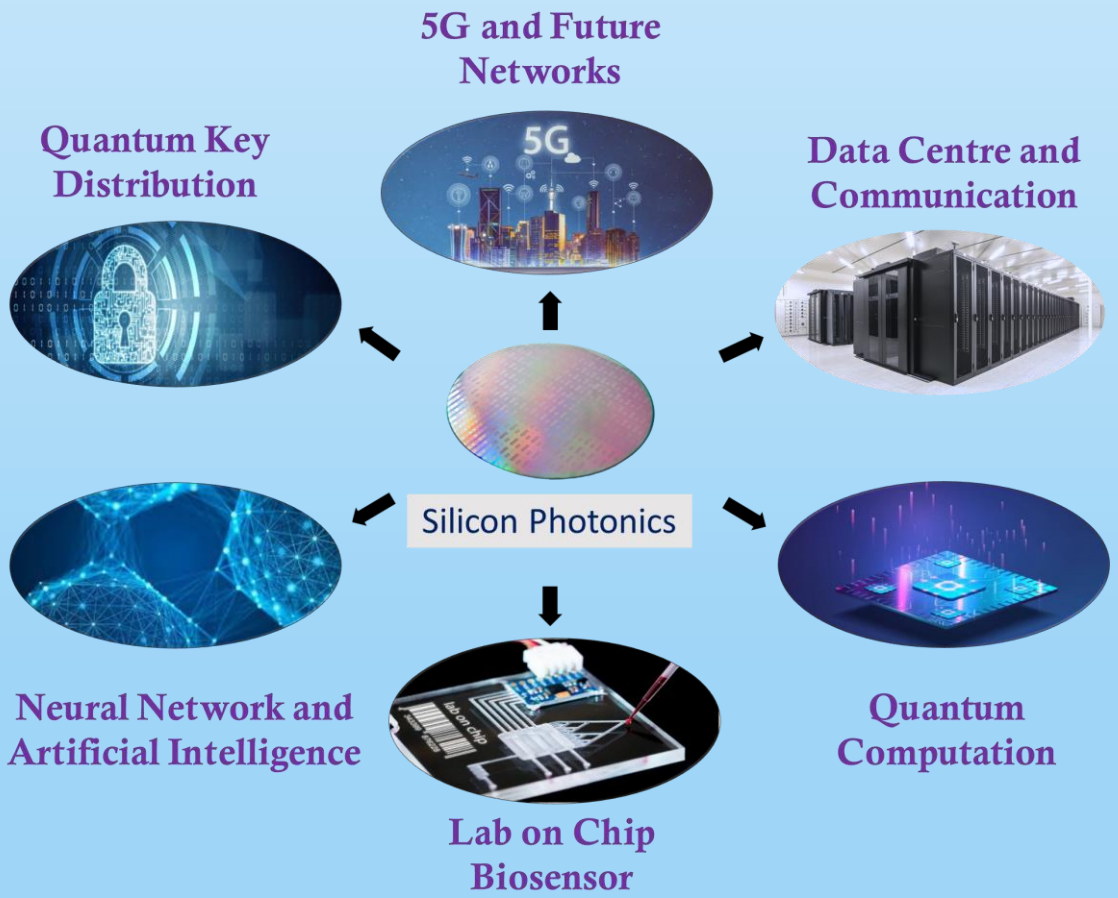
2006 → 2022

- 2006 — Establishment of Integrated Optoelectronics Lab (IIT Madras Seed Funding Rs. 5L)
- 2008 — First funded projects on Silicon Photonics (DRDO, DST, DIT)
- 2009 — Demonstration of 5 µm SOI optical waveguide
- 2010 — First MS thesis on Silicon Photonics
- 2011 — Demonstration of packaged Silicon Photonics devices (5 µm SOI)
- 2012 — Funding for Silicon Photonics Nanotechnology (CNNP/MeitY, DRDO)
- 2013 — Demonstration of Silicon Photonics active devices (PIN waveguide, 5 µm SOI)
- 2014 — Demonstration of spot size converter (Microns to sub-micron waveguides)
- 2015 — Demonstration of surface trimming of devices using controlled RIE
- 2016 — First international patent filed, first PhD graduation
- 2017 — First publication on CMOS compatible Silicon Photonics devices (220 nm SOI)
- 2018 — Demonstration of CMOS compatible reconfigurable Silicon Photonics devices
- 2019 — Demonstration of FWM in Silicon photonic wire waveguide devices
- 2020 — Demonstration of high extinction on-chip pump rejection filters
- 2021 — 6 PhD and 15 MS Graduated; IoE-pCoE; MeitY CoE-CPPICS

Present Status: 4 Research Associates, 12 Ph.D., 3 MS Scholars, and 10 Project staffs

Current Research Activities

Present research focus of the CPPICS team is mainly centering around design, demonstration and packaging of photonic chips for advanced microwave and quantum photonic applications.



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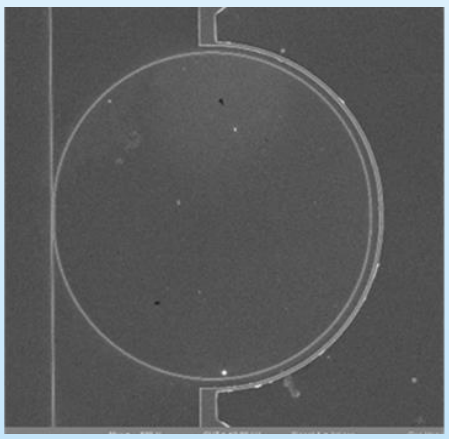
Technology Platform

CMOS compatible silicon photonics technology is our overall driving force. In general, there are two types of optical waveguide cores used for silicon photonic integrated circuits: (i) Si photonic wire waveguides in SOI and (ii) SiN waveguides on the surface of oxide grown bulk silicon substrate. We have already developed state-of-the-art SOI based silicon photonics technology over the years and very recently started working on developing SiN waveguide process technology. We are also open to access commercial silicon photonics foundries through multi-project wafer (MPW) runs.

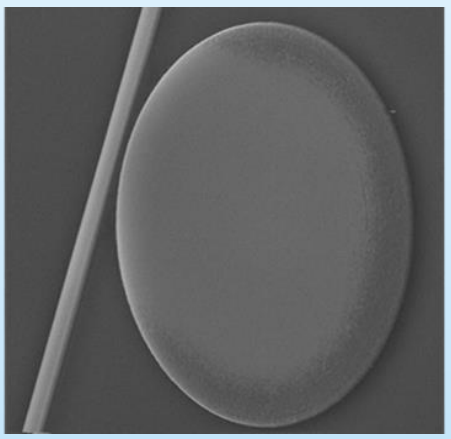
Silicon Waveguide Technology (In-house)

Some of our fabricated high performance devices are Microring Resonators (MRRs), Distributed Bragg Reflectors (DBRs) based High Extinction Pump Rejection Filters, Wavelength Independent Power Splitters, Programmable MRRs for Photon Pair Generation, MZI based Programmable Tunable Basic Units (TBUs)

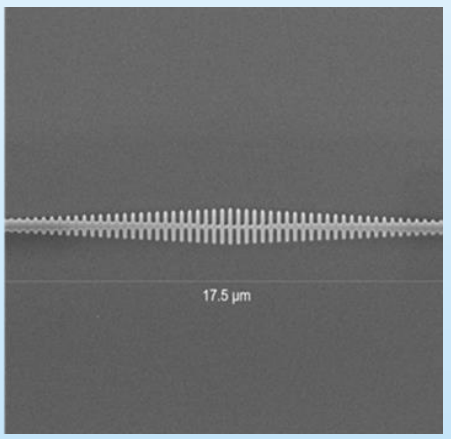
Tunable Microring Resonator



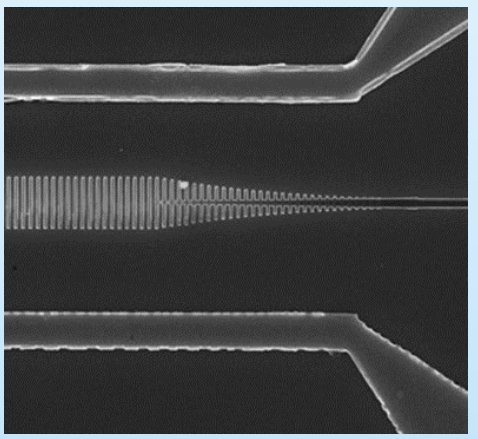
Disk Resonator



Broadband DBR stopband Filter

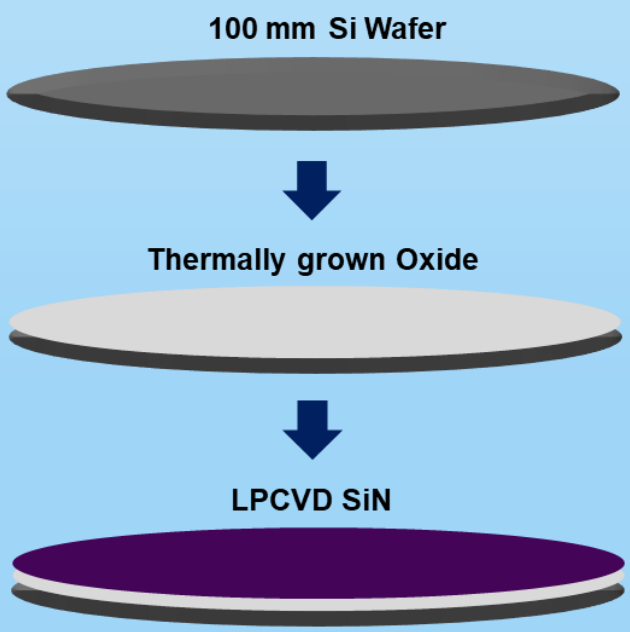


Tunable SWG Waveguide

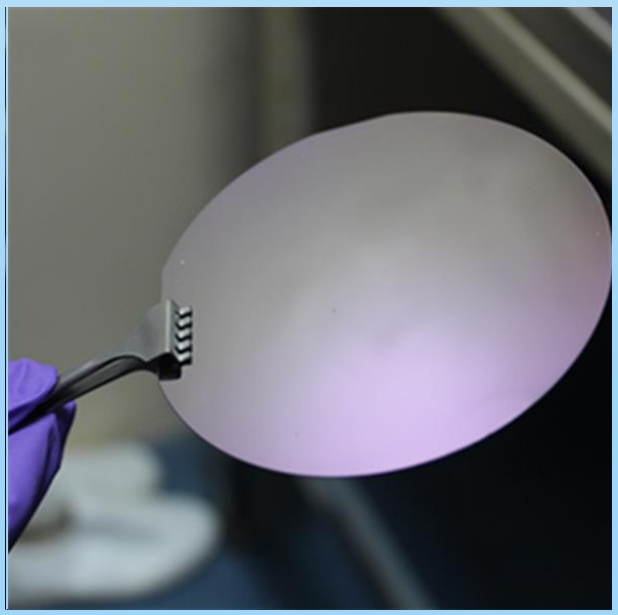


Silicon Nitride Waveguide Technology (In-house)

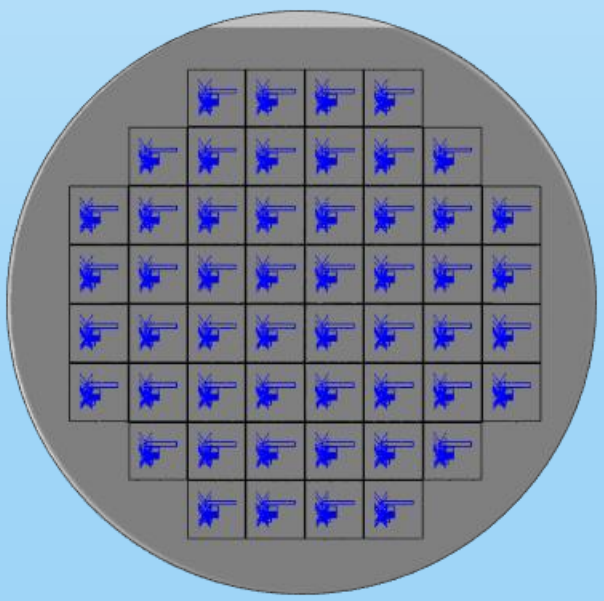
The deposition of stoichiometric silicon nitride film has been optimized using LPCVD on a 4 inch wafer with a thickness up to 400 nm with less than ±2 % variation. We aim to demonstrate low loss silicon nitride based photonic devices for different applications in Microwave and Quantum photonics.



In-house Fabricated SiN Wafer



Wafer Scale Process Development



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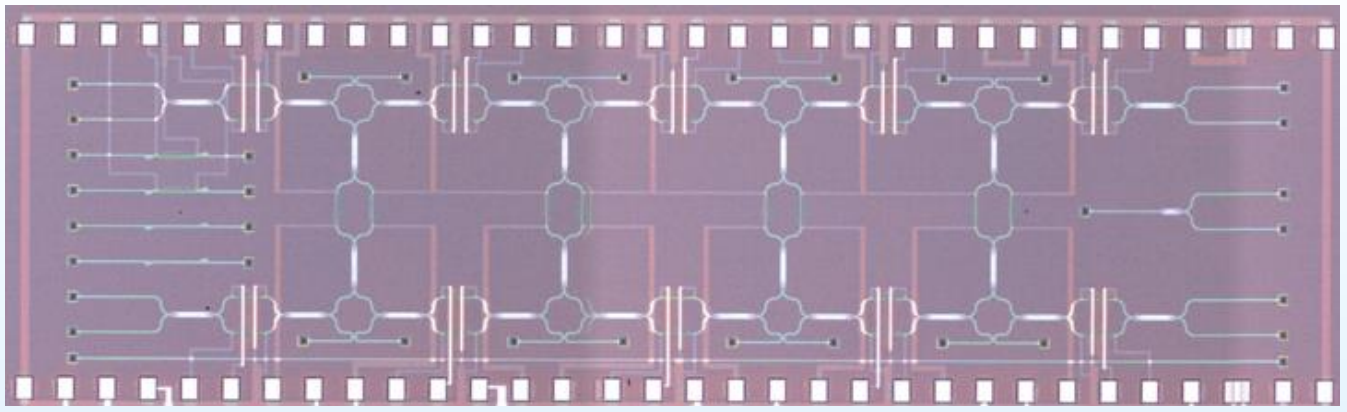
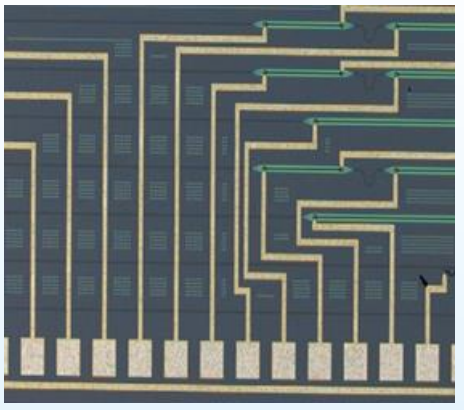
Circuit Design & Demonstration through MPW Runs

Tape-out from IMEC, Belgium

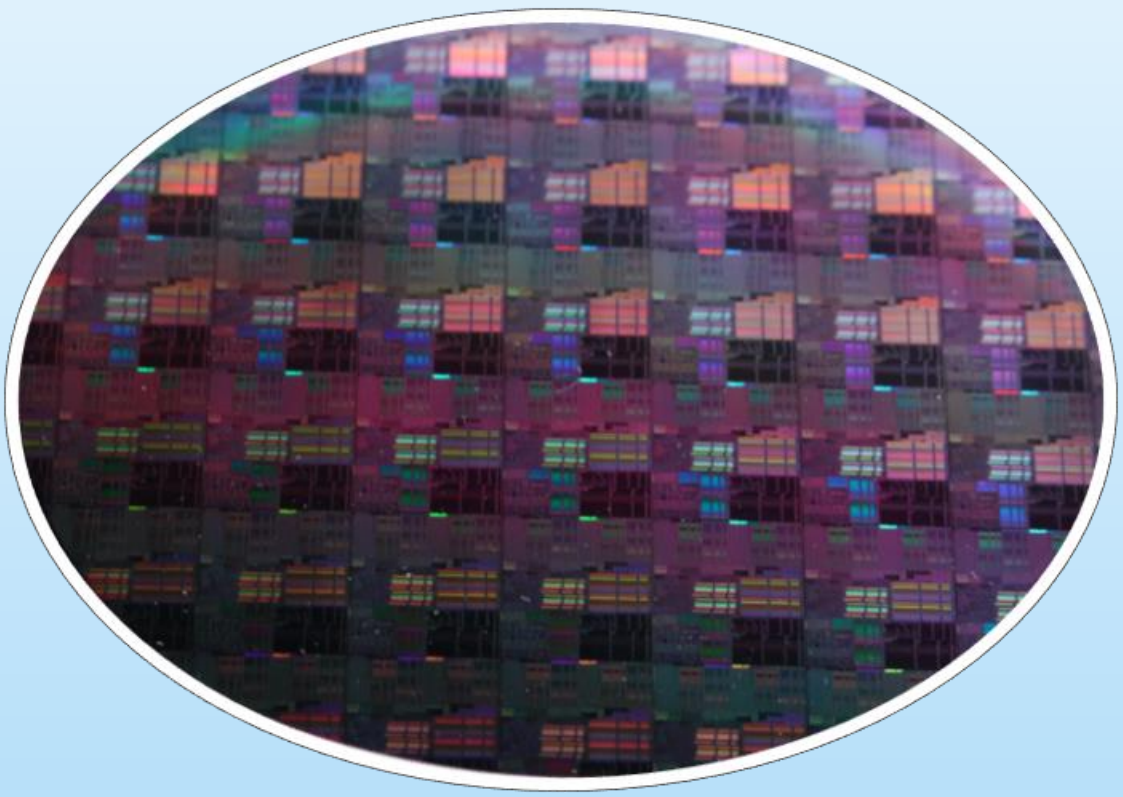


Tape-out from AMF, Singapore

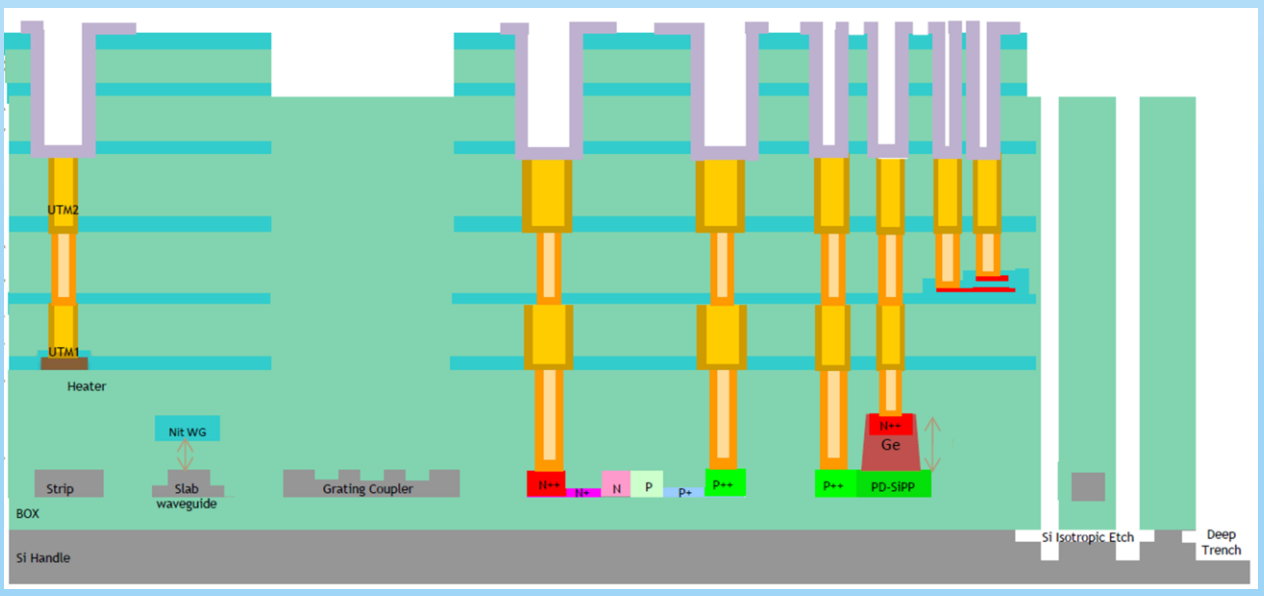


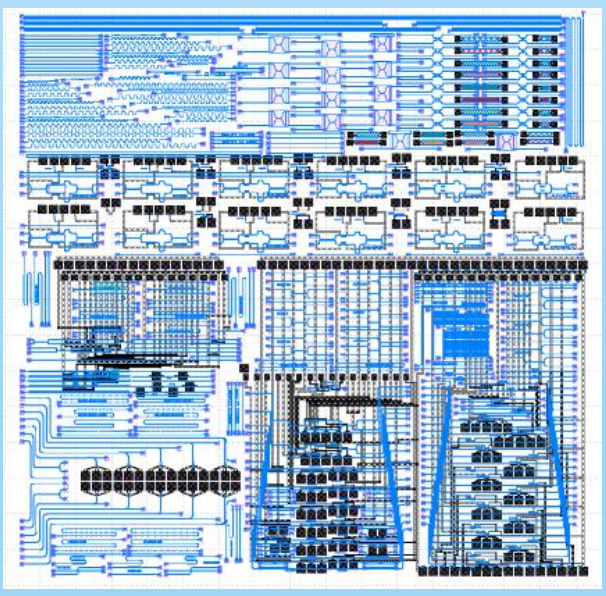
PDK Development for Silicon Photonics Technology with SilTerra, Malaysia

200 mm Wafer Processed at SilTerra, Malaysia



Passive & Active Component Design Layout for Foundry Tapeout by Team CoE-CPPICS





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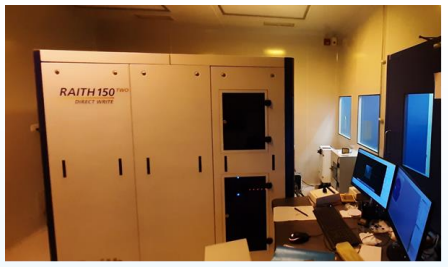
Photonic Chip Design, Fabrication & Characterization:



Cleanroom facilities spreading over 5000 Sq.ft.

Major Process Tools for Silicon Photonics:

- ❑ E-Beam Lithography
- ❑ DUV and i-line Lithography Systems
- ❑ Laser Mask Writer
- ❑ ICP RIE and Deep RIE Systems
- ❑ Metallization and Sputtering Units
- ❑ LPCVD and PECVD Systems
- ❑ Oxidation and Diffusion Furnaces
- ❑ Chemical Mechanical Polishing (CMP)

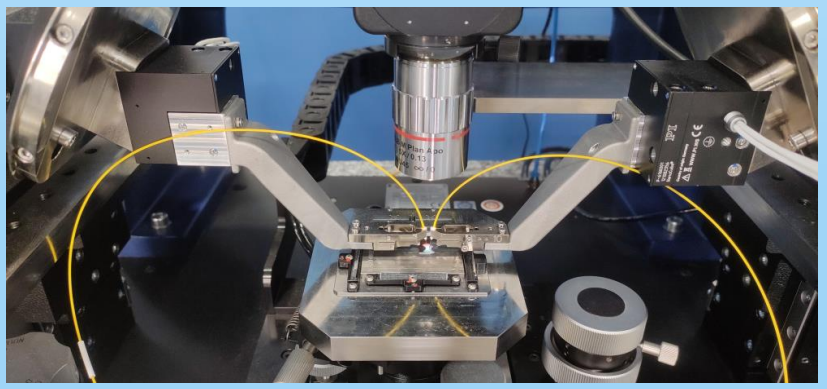
2500 sq. ft. of Design and Characterization Labs

Design & Simulation Tools:

- ❑ Ansys Lumerical
- ❑ Cadence Photonics
- ❑ COMSOL Multiphysics
- ❑ Synopsys Sentaurus

Major Characterization Tools:

- ❑ Wafer-scale silicon photonics probe station
- ❑ Indigenous chip-scale silicon photonics probe station
- ❑ Superconducting Nanowire Single Photon Detector Systems
- ❑ Light Component Analyzer and Vector Network Analyzer
- ❑ High Resolution Optical Spectrum Analyzer
- ❑ Fiber Pigtailing and Packaging Setup
- ❑ Real-time Digital Oscilloscope
- ❑ Arbitrary Waveform Generator



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Photonic Chip Assembly & Fiber Attachment:

We are in a process of developing state-of-the-art photonic chip assembly and fiber attachment facilities. Some of our commissioned facilities and indigenous setup under development have been highlighted here.

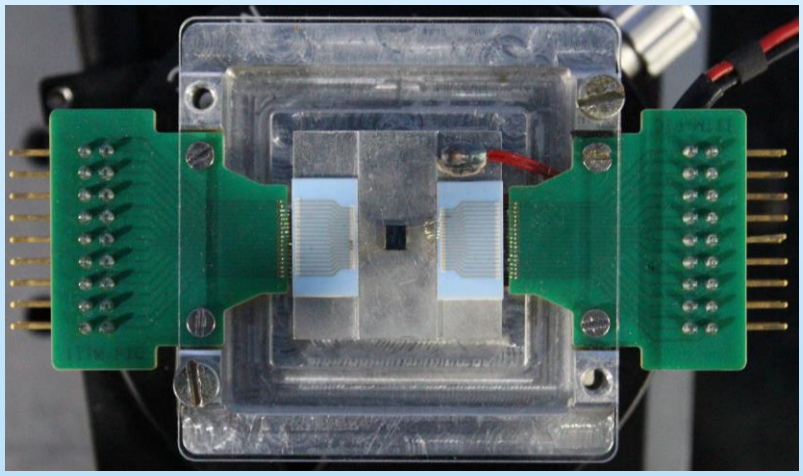
Wafer Planarization (Upto 100 mm wafer)

Wafer Dicing Machine (upto 150 mm wafer)

Waveguide Edge Polishing System (upto 0.1 µm)

Wire Die Bonder (Up to 25 Mil)

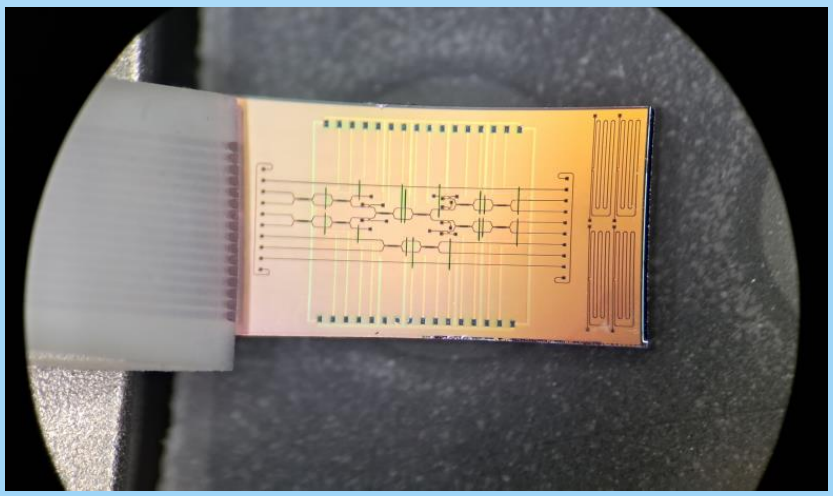
2nd Iteration of Photonics Chip Packaging

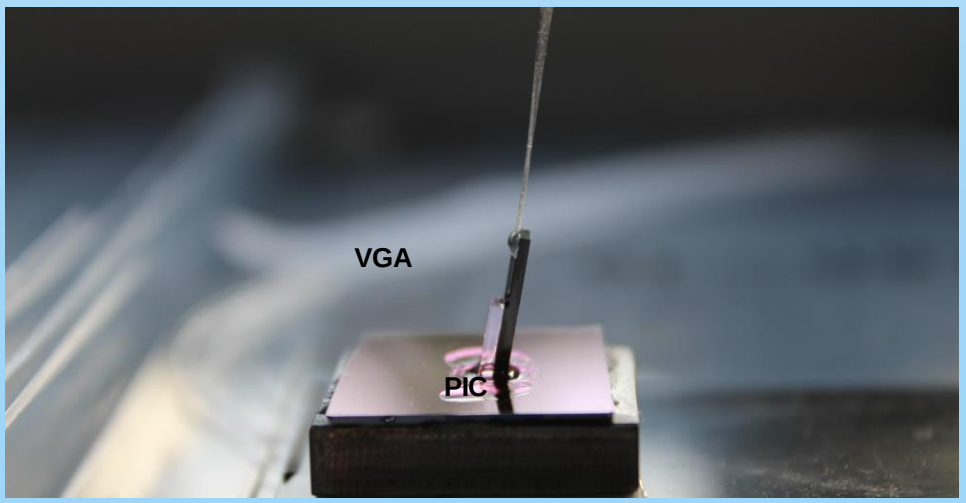


Photonic packaging and assembly is a complex and multi-disciplinary design and manufacturing process. To make a PIC-enabled module to perform according to specification, sub-micron precision alignment and bonding process are required. At the same time, precise thermal management is required to maintain the thermo-optic stability of the signals. We have collaborated ourselves with Si2 Microsystems, a company that works in the development of packaged integrated circuits, to overcome the existing limitations.

In-house Packaging setup & attached PIC with V-groove array

Our indigenous setup to couple light from/to optical fiber or V-Groove Array (VGA) to/from a photonic chip, where VGA is an array of optical fibers placed together with precise spacing so that we can couple light to/from the photonic chip at multiple optical inputs/outputs simultaneously. Using this setup one can precisely place a VGA on its holder set up so that it can be aligned with the photonic chip with the sub-micron level of precision for optical i/o coupling.





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Chief Investigator:

Dr. Bijoy Krishna Das
Professor in Electrical Engineering
Expertise : Silicon Photonics

Chief Technology Officer:

Mr. Arnab Goswami
Expertise : Silicon Photonics
Email: cto-cppics@ee.iitm.ac.in

Co-Investigators:

Dr. Amitava DasGupta
Professor in Electrical Engineering
Expertise : Device Modeling & VLSI Technology

Dr. Anil Prabhakar
Professor in Electrical Engineering
Expertise : Quantum Photonics

Dr. Anjan Chakravorty
Professor in Electrical Engineering
Expertise : Compact Modeling

Dr. Deelep R. Nair
Professor in Electrical Engineering
Expertise : Design, Fab and Testing

Dr. Deepa Venkitesh
Professor in Electrical Engineering
Expertise : Fiber Optics & RF Photonics

Dr. Enakshi Bhattacharya
Professor in Electrical Engineering
Expertise : MEMS & Photonics

Dr. Janakiraman Viraraghavan
Asst. Professor in Electrical Engineering
Expertise: Circuit Design, Fab and Testing

Dr. Nandita DasGupta
Professor in Electrical Engineering
Expertise: Microelectronics & Photonics

Dr. Sargunaraj Christopher
Professor in Electrical Engineering
Expertise : Microwave Engineering

Dr. Sudharsanan Srinivasan
Asst. Professor in Electrical Engineering
Expertise : Photonics/Si Photonics Technology

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Industry Advisory Board :

CHAIRMAN

Dr. Mallik Tatipamula

CTO at Ericsson
San Jose, California, USA

Message from the Chairman-

I am delighted that the Centre of Programmable Photonic Integrated Circuit & Systems (CPPICS) has been engaged with cutting edge technology R & D activities under the leadership of Prof. Bijoy Krishna Das. The progress of CoE-CPPICS has been commendable during the last couple of years and its future R&D roadmap has been well planned complying with the immediate needs of silicon photonics/electronics industries. As the chairman of CPPICS Industry Advisory Board, I am committed to coordinate with other board members to provide guidance to the team CoE-CPPICS to continue its activities following the Product Research Development and Manufacturing Model.

MEMBERS

Dr. Vivek Raghunathan

Founder & CTO
Xscape Photonics Inc., USA

Mr. Arjun Kumar Kantimahanti

Senior Vice President
SilTerra, Malaysia

Dr. Prith Banerjee

CTO, Ansys Inc.
Palo Alto, California, USA

Mr. Kailash Narayanan

President and General Manager
Keysight Technologies, USA

Mr. Vijay Janapaty

Vice President and General Manager
Broadcom Inc., USA

Dr. Steve Johnston

Vice President
Merck KGaA Darmstadt, Germany

Dr. Ravi M. Bhatkal

Managing Director
India Element Solutions Inc, India

Mr. Dinanath Soni

Executive Director,
Si2 Micro System, India

Mr. Vikas Gupta

Senior Director
GlobalFoundries USA

Mr. Narayan Srinivasa

Director
Intel Corporation USA

Dr. Kishore Kamath

Vice President and General Manager of R&D
Intel Corporation USA

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Industry Collaborators:

Foundry Partner

SILTERRA, Malaysia is our Silicon Photonics foundry partner. We have been committed for a joint R&D on Silicon Photonics technology and various applications. Team CoE-CPPICS will contribute with component design, characterizations and compact modelling towards Process Design Kit block development.

Photonics Chip Packaging Partner

Si2 Microsystems is the hi-tech semiconductor and systems company specializing in miniaturization using System-in-Package, with India based facilities for 3D packaging. To get a clear perspective about industry demands and to keep up with the needs of the Silicon Photonics market, we have collaborated with Si2 Microsystems to bring system-in-package solutions for photonic integrated circuits.

Modeling and Testing Partner

Keysight Technologies USA and CoE-CPPICS have signed MoU to establish an advanced silicon photonics chip testing facility at IIT Madras and exploring together on innovative solutions for electronic-photonic design automation.

Academic Collaborators :

In pursuit to maintain our high standards of research and development in the field of Silicon Photonics, we have stepped forward to link up with renowned researchers from all around the world. Such collaborations come useful while exchanging ideas and knowledge with various research groups in our field. CoE-CPPICS has been immensely benefitted in its formation from the following three pioneer figures:

Prof. Shayan Mookherjea
University of California San Diego, USA

Prof. Wim Bogaerts
Ghent University/IMEC, Belgium

Prof. Jose Capmany
University of Valencia, Spain

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Services & Training Objectives

Scan Here to Know More

We are expecting following services for external users by the end of 2023:

- ❑ Consultancy services for Photonics Chip Design and Fabrication
- ❑ Hands-on Training for Photonics Device Design and Fabrication
- ❑ Photonic IC Fiber Pigtailing and Packaging Services
- ❑ Workshops/Short-Term Courses on Integrated Photonics

Please feel free to contact us for any service related queries to admin@cppics.iitm.ac.in

Feedback from our PhD Graduates

Dr. Riddhi Nandi
Graduation Year: 2021
Principal Design Engineer
Global Foundries Pvt. Ltd, India

"The learning obtained during fabrication; characterization provides an edge over others"

Dr. Sumi Radhakrishnan
Graduation Year: 2020
R&D Engineer
IMEC Belgium

"I feel privileged to use the state-of-the-art CNNP facilities as part of my PhD program".

Dr. Ramesh Kudalippalliyalil
Graduation Year: 2019
Postdoctoral Research Associate
University of Maryland, USA

"It was amazing and unique research experience with a supporting team and well-developed infrastructure."

Dr. Parimal Sah
Graduation Year: 2018
Assistant Professor
Bhagalpur College of Engg. , India

"Working in CPPICS helped me to learn design, simulation, fabrication and characterization of integrated optoelectronic devices"

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Dr. Sujith Chandran
Graduation Year: 2017
Research Engineer (ISI)
University of Southern California, USA

"I feel honored to be the part of CPPICS, great work culture and an Ideal group to learn from the fundamentals"

Dr. Shantanu Pal
Graduation Year: 2016
Principal Design Engineer
Global Foundries Pvt. Ltd, India

"It was a great experience in CPPICS – learned how to do research starting from building experimental lab to publish papers in international journals."