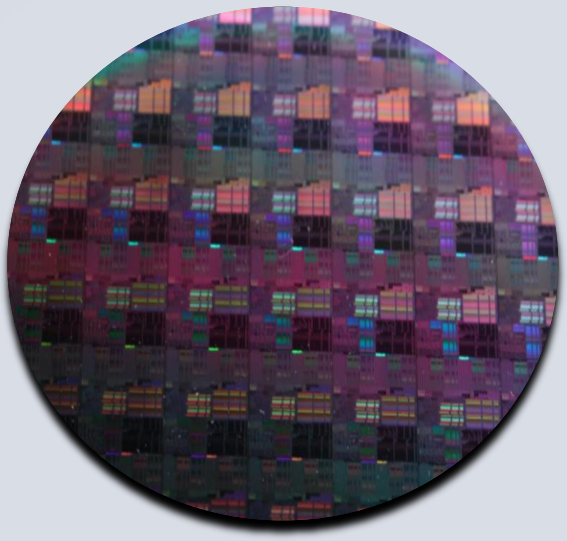
Silicon Photonics CoE-CPPICS

Technical Digest



Inaugural Edition
20th October 2023

MAKE IN INDIA

Department of Electrical Engineering
IIT Madras, Chennai – 600 036
Website: https://cppics.iitm.ac.in/

MeitY
Government of India

Preface

I am delighted to write the preface for the 1^{st} edition of the Technical Digest of our Silicon Photonics Centre of Excellence: The Centre for Programmable Photonic Integrated Circuits and Systems, which is fondly known as Silicon Photonics CoE-CPPICS. I am more so happy that this technical digest is being released by the Hon'ble Secretary, Shri S. Krishnan (IAS, TN'89), Ministry of Electronics and Information Technology (MeitY), Govt. of India in the august presence of our Hon'ble Director Prof. V. Kamakoti; the Dean of IC&SR Prof. Manu Santhanam; the Head of Electrical Engineering Dept. Prof. Nagendra Krishnapura; the R&D Group Coordinator (MeitY, Govt. of India) Smt. Sunita Verma; the Vice President of R&D, Intel Silicon Photonics Product Division, Dr. Kishore Kamath; and last but not the least Dr. Sankhadip Das, Scientist 'D' (MeitY, Govt. of India) who was instrumental in supporting to establish a Silicon Photonics Centre of Excellence at IIT Madras, by pursuing his senior scientists Dr. Sandip Chatterjee and others.

The purpose of releasing this 1^{st} edition of Silicon Photonics CoE-CPPICS Technical Digest is to capture the present infrastructure & facilities as well as the R&D progress of the centre that has taken place since its inception in 29^{th} December 2020 (Sanction Order: GG-11/15/2020-EMCD, dated 29.12.2020). Our Chief Technology Officer, Arnab Goswami and senior research scholar Ashitosh Velamuri have put up a huge effort to coordinate with other research scholars and postdoctoral research associates in helping topic-wise technical writeups as well as editing in its present form. I am also grateful to my faculty colleagues Prof. Enakshi Bhattacharya, Prof. Nandita DasGupta, Prof. Amitava DasGupta, Prof. Anil Prabhakar, Prof. Anjan Chakravorty, Prof. Deleep Nair, Prof. Deepa Venkitesh, Prof. Janakiraman Viraraghavan, Prof. Sankaran Aniruddhan, and Prof. Sudharsanan Srinivasan who have been associated with our Silicon Photonics CoE-CPPICS and guiding our research scholars with in the scope of its deliverables, growth and sustenance. I also put on record the contribution of our senior distinguished colleague Prof. S. Christopher (Ex-Chairman, DRDO), who helped us framing user oriented various research proposals including the Silicon Photonics CoE-CPPICS itself. Most importantly, because of his initiative we found most trusted industry collaborator Mr. Dinanath Soni, Executive Director of Si2 Microsystems Bangalore.

Besides, I am enormously grateful to our Director Prof. V. Kamakoti who have been supporting our Centre to be flourished with additional financial supports from the IIT Madras Institute of Eminence grant. With his far-sight vision, Prof. Kamakoti encouraged us to form an Industry Advisory Board for our Silicon Photonics CoE-CPPICS. Today, we have a very active CPPICS Industry Board, chaired by Dr. Mallik Tatipamula (CTO at Ericsson, Silicon Valley, USA), for guiding us to carry out industry relevant R&D activities. The other distinguished members in our CPPICS Industry Advisory Board are semiconductor industry leaders like Dr. Vivek Raghunathan (Xscape Photonics, USA), Dr. Kishore Kamath (Intel USA), Dr. Steve Johnston (Merck KGaA, Germany), Dr. Prith Banerjee (Ansys USA), Dr. Ravi M. Bhatkal (India/USA Element Solutions), Mr. Narayan Srinivasan (Intel USA), Mr. Vijay Janapaty (Broadcom Inc., USA), Mr. Vikas Gupta (GlobalFoundries, USA), and Mr. Dinanath soni (Si2 Microsystems, India). Because of their collective efforts and support, the Team Silicon Photonics CoE-CPPICS has signed R&D MoU with Si2 Microsystems, Bangalore and Keysight USA. We are also actively engaged in R&D collaboration with Silterra Malaysia and are in the process of signing R&D MoU. We are expecting many more such R&D MoUs in coming years. Our Dean IC&SR, Prof. Manu Santhanam also deserves a huge applause for extending all sorts of administrative supports to run our Silicon Photonics CoE-CPPICS. I also take this opportunity to thank Prof. David Koilpillai (Head of the EE Dept. at the time of centre's inception) and Prof. Nagendra Krishnapura (current Head of the EE Dept.) for their constant supports and encouragements, especially, allocating lab spaces on time and facilitating department utilities.

Finally, I must acknowledge our centre administrative and maintenance support team Ms. Sindhura Balaraman, Mr. Inba Sekaran and Mr. Mohan Babu who have been playing pivotal roles

for running the lab on day-to-day basis. I also extend my sincere appreciation to our Centre for NEMS and Nano Photonics (CNNP) staff Dr. Srinavasa Reddy, Mr. Rajendran C, Mr. Prakash J, Mr. Venkateswaran G, Ms. Vani Ms. Amudha G, Mr. Muthaiah M and Mr. Sridhar T for their hard work in running CNNP facilities and helping hands for establishing our Silicon Photonics CoE-CPPICS Labs. The fab facilities in CNNP are extensively used for our in-house silicon photonics technology research. Lastly, but not the least, I fondly remember all our former students, research scholars and project staff who contributed over the years, making IIT Madras proud today on the eve of the inaugural ceremony of our fully functional Silicon Photonics CoE-CPPICS, the first of its kind in India and perhaps elsewhere in the world.

In summary, I wish the Silicon Photonics CoE-CPPICS to play a major role in the upcoming years to reduce the existing gaps in the country and fulfill the ambitious objectives of India Semiconductor Mission announced by the Govt. of India and looking forward to the next edition of Silicon Photonics CoE-CPPICS Technical Digest in 2024 with much more global visibility.

Sincerely,

(Bijoy Krishna Das)
Chief Investigator, Silicon Photonics CoE-CPPICS

Date: 20th October, 2023

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The Hon'ble Secretary, MeitY, Govt. of India

एस. कृष्णन, आई.ए.एस.
सचिव
S. Krishnan, I.A.S.
Secretary

सत्यमेव जयते

इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी मंत्रालय
भारत सरकार
Ministry of Electronics &
Information Technology (MeitY)
Government of India

MESSAGE

Digital India, a flagship program of the Government of India has catalysed the country's transformation into a digitally-empowered society and knowledge economy. The Photonic Integrated Circuit (PIC) which can be used to create faster and more energy-efficient devices for data processing and digital computing is expected to dominate market requirements in various sectors in the next decade. Some of these sectors include Data and Telecommunications, Healthcare and Medicine, Automotive and Engineering and so on. PICs are also very useful for ambient temperature and affordable quantum technologies.

Ministry of Electronics and Information Technology (MeitY) is currently supporting the development of various PIC technology platforms such as silicon photonics, diamond photonics, polymer photonics and lithium niobate photonics along with PIC packaging technologies through its self-sustainable R&D centres which operate in PPP mode supporting "Atmanirbhar Bharat" mission of Govt. of India.

MeitY has initiated a Centre for Programmable Photonic Integrated Circuit and Systems (CPPICS) at IIT Madras in collaboration with industry to design, manufacture and develop applications based on Field Programmable Photonic Gate Array (FPPGA) cores using Silicon Photonics, in December 2020. The centre is slated to become self-sufficient in 5 years' time, commercialize the products through Start-up and train manpower to boost the eco-system of PIC manufacturing in India. The centre is collaborating with M/s Si2 Microsystems, Bangalore for System-in-Package solutions for the proposed silicon photonics FPPGA cores. This technology is expected to serve multiple sectors with multiple applications such as quantum computing, quantum communication, 5G/6G communications, IoT, radar & avionics and so on.

I extend my congratulations to the CPPICs team, IIT Madras, and the MeitY team for their diligent efforts in establishing the centre and advancing its objectives.

I wish the centre great success in taking the technology to its full commercialization and starting PIC manufacturing in India.

(S. Krishnan)

Place: New Delhi
Dated: 17.10.2023

आज़ादी का अमृत महोत्सव

Digital India
Power To Empower

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चेन्नै – ६०० ०३६

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प्रो. वी. कामकोटि
Prof. V. Kamakoti
निदेशक
Director

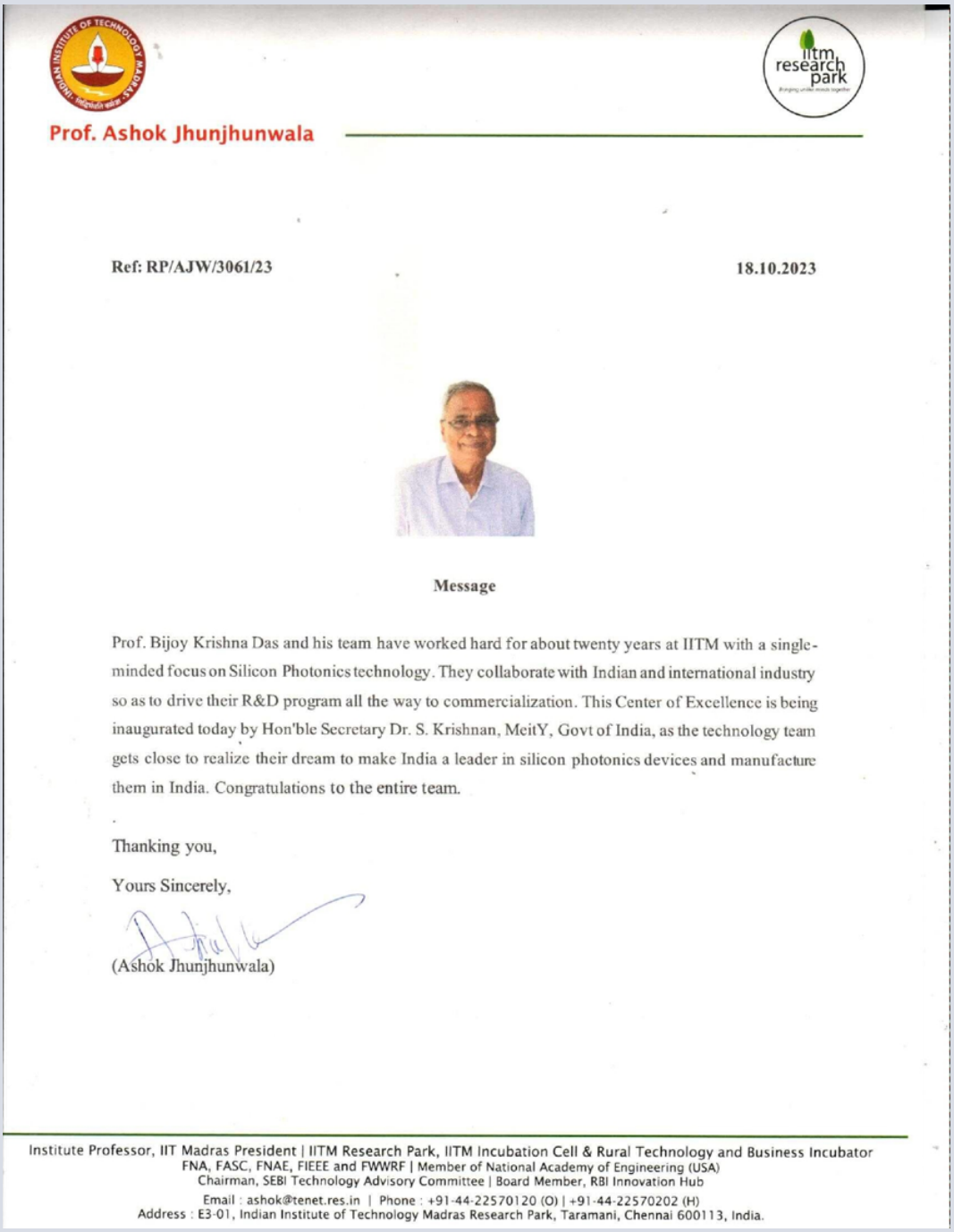
MESSAGE

As our Country is moving towards building our own capability in the area of semiconductor electronics, it is very heartening to see our Institute establish a Centre of Excellence in Silicon Photonics, which is an outcome of extensive R & D pursued over nearly two decades. The substantial seed funding for establishing this state-of-the-art *Silicon Photonics Centre of Excellence on Programmable Photonic Circuits and Systems (CPPICS)* by the Ministry of Electronics & Information Technology (MeitY), Govt. of India has helped in the consolidation of indigenously developed silicon photonics technology at IIT Madras. In addition, I am glad to welcome a distinguished Advisory Board comprising global industry leaders from Ericsson, Broadcom, Keysight, Intel, Global Foundries, Silterra, and others. I have no doubt that this board will mentor the CoE-CPPICS team to execute its R & D program oriented towards product research and development and link the same with an effective manufacturing model. I am more so happy to note that the CoE-CPPICS labs are now fully equipped with high-end characterization and testing facilities for silicon photonics devices and circuits; both at die-level and wafer level. My heartiest congratulations to the entire R&D team of CPPICS headed by Prof Bijoy Krishna Das, on this inauguration day when the Centre is to be dedicated to the Nation. I am confident that the Centre is going to impact significantly, both in the domestic as well as global silicon photonics R & D market in the upcoming years.

V. Kamakoti

V. Kamakoti

Director of IIT Madras Research Park



Prof. Ashok Jhunjhunwala

Ref: RP/AJW/3061/23 18.10.2023

Message

Prof. Bijoy Krishna Das and his team have worked hard for about twenty years at IITM with a single-minded focus on Silicon Photonics technology. They collaborate with Indian and international industry so as to drive their R&D program all the way to commercialization. This Center of Excellence is being inaugurated today by Hon'ble Secretary Dr. S. Krishnan, MeitY, Govt of India, as the technology team gets close to realize their dream to make India a leader in silicon photonics devices and manufacture them in India. Congratulations to the entire team.

Thanking you,

Yours Sincerely,

(Ashok Jhunjhunwala)

Institute Professor, IIT Madras President | IITM Research Park, IITM Incubation Cell & Rural Technology and Business Incubator
FNA, FASC, FNAE, FIEEE and FWWRF | Member of National Academy of Engineering (USA)
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Dean of IC&SR, IIT Madras

Office of Industrial Consultancy & Sponsored Research (IC&SR)
INDIAN INSTITUTE OF TECHNOLOGY MADRAS
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Professor Manu Santhanam
DEAN, IC & SR

MESSAGE

It gives me immense pleasure to see the launch of the MEITY Centre of Excellence on Programmable Photonic Integrated Circuits and Systems (CPPICS). IIT Madras has had a long and successful partnership with MEITY, and the CoE will be another landmark in this collaboration. The activities of the centre will significantly impact the country's focus on AI and quantum computing. With its excellent faculty expertise and facilities, IIT Madras is geared to drive the research efforts in the area of silicon photonics, which is a core aspect of these domains. I wish the team in the Department of Electrical Engineering at IIT Madras all the very best in this endeavour.

Dr. Manu Santhanam

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Head, Dept. of Electrical Engineering, IIT Madras

Indian Institute of Technology Madras
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Nagendra Krishnapura
Professor and Head
Department of Electrical Engineering

नागेंद्र कृष्णपुरा
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Electronic circuits with nonlinear active devices were born in the early twentieth century. They gradually became more complex as their components evolved from vacuum tubes to transistors. However the key enabler of the exponential growth of circuits over the last half century is monolithic integration. Photonic circuits have been around for a century, and optical fibre communication circuits with lasers for half a century. They are now poised for exponential growth aided by monolithic integration. Photonic components have been integrated to a limited extent on various materials over the last three decades. The recent advent of silicon photonics is expected to accelerate their growth substantially. Silicon photonics enjoys the twin advantages of being integrable with electronic circuits on silicon and being able to leverage the decades-long research on the silicon integrated circuit. The inherently wide bandwidth of photonic communication is key to fulfilling our ever-increasing appetite for data. The Centre of Excellence on Programmable Photonic Circuits and Systems (CPPICS) at IIT Madras, funded by the Ministry of Electronics & Information Technology (MeitY), Govt. of India, will be a driver of this exciting area. It benefits from the participation of faculty with a strong background in devices, circuits, and communication systems. With its potential for innovation and skilled workforce development in photonic IC technology and circuits, the centre serves as a springboard for the country to dive into photonic integration in its early days and be a leader instead of a follower.

CTO, Ericsson, Silicon Valley, USA

ERICSSON

October 11, 2023

I am delighted that the Centre of Programmable Photonic Integrated Circuit & Systems (CPPICS) has been engaged with cutting edge technology R&D activities under the leadership of Prof. Bijoy Krishna Das. The progress of CoE-CPPICS has been commendable during the last couple of years and its future R&D roadmap has been well planned complying with the immediate needs of silicon photonics/electronics industries.

As the chairman of CPPICS Industry Advisory Board, I am committed to coordinate with other board members to provide guidance to the team and support centre activities following the Product Research Development and Manufacturing Model. Over the past few months, centre has made tremendous progress in establishing industry partnerships and MoUs with Keysight technologies, ANSYS, Silterra, and hope to see even more industry engagements in coming months. Congratulations to the CPPICS team, as your research has and will continue to bring about great change in the world, and your recent achievements are a great testament to the spirits of inquiry and scientific discovery.

On behalf of industry advisory board, I would like to take this opportunity to thank CPPICS team for your dedication and contributions. It's inspiring to see all your hard work paying off, and we are excited to continue this journey with you, and best wishes to you all in future endeavors.

With best wishes,

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VP of R&D, Intel Silicon Photonics Product Div., USA

MESSAGE

We are on the cusp of the evolution of Semiconductor Photonics Technologies, transitioning from a relatively esoteric niche to becoming a core technology in some of the fastest-growing industries. Optical networking has become the backbone of data center connectivity. High-capacity interconnects are required to move vast amounts of data among compute, memory, graphics nodes, and AI clusters within the data centers, as well as to transfer data in and out of mega data centers. Silicon Photonics has emerged as the technology of choice for such applications due to its ability to integrate Photonic components on the Silicon platform, thereby leveraging the maturity, high volume, and cost benefits of traditional Silicon Fab. Silicon Photonics is also expanding into newer applications such as LiDAR and sensors for automotive and consumer applications.

The establishment of the Center of Excellence in Silicon Photonics at IIT Madras is an excellent opportunity for researchers to lead the innovation and exploration of new frontiers in this emerging technology. The Center for Programmable Photonics Integrated Circuits and Systems (CPPICS), under the leadership of Prof. Bijoy Krishna Das, is conducting cutting-edge research in this field. The team has published scientific papers in reputable journals and conferences. As a member of the Industry Advisory Board, I believe there are opportunities for CPPICS to collaborate with the industry in various areas. These opportunities include developing innovative solutions through design, modeling, and simulation, as well as performing complicated and intense tests and characterizations to address challenging technical issues.

I would like to congratulate CoE-CPPICS on the successful launch and the progress made thus far in such a short time. I am confident that the team will achieve great success in scientific research in Silicon Photonics.

Kishore Kamath, PhD

VP of R&D, Silicon Photonics Product Division

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Executive Director, Si2 Microsystems, Bangalore

Si2 microsystems™
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To,

Team Silicon Photonics,
COE-CPPICS – IIT - Madras

On behalf of Si2 Microsystems Pvt. Ltd., I am delighted to extend our most sincere congratulations on the inauguration of the Centre of Excellence at Centre for Programmable Photonic Integrated Circuits and Systems at IIT Madras!

This momentous occasion marks a significant milestone not only for the academic community but also for the broader industry. We are immensely proud and excited to be part of this collaborative venture, which promises to be a cornerstone of innovation and technological advancement in the field of photonic integrated circuits.

As an industry partner, we deeply appreciate the vision and dedication that have gone into establishing this center. It is a testament to the pioneering spirit of IIT Madras and the commitment to fostering cutting-edge research and development. We are confident that this collaboration will lead to breakthroughs in technology and applications that will reshape industries and improve lives.

The research, expertise, and innovation that will emanate from the Centre for Programmable Photonic Integrated Circuits and Systems are poised to revolutionize the way we think about and utilize photonic technologies. It is with great anticipation that we look forward to the discoveries and advancements that will undoubtedly emerge from this hub of knowledge and collaboration.

It has been an arduous journey during the Covid times with equipment supply positions being difficult. Despite the setbacks the progress from the fabrication and characterization of the simple elements to complex structures and onwards to our first integrated photonics circuit – the QKD Transceiver Chip, being delivered on schedule by December 2023.

We are excited to be a part of this journey, working hand in hand with the brilliant minds at IIT Madras to shape the future of photonic integrated circuits and systems. Together, we can explore uncharted territories and bring about transformative changes.

Once again, congratulations on this remarkable achievement, and we eagerly await the possibilities that this center will unfold. The road ahead is filled with promise, and we are honored to be part of this extraordinary venture.

Best wishes

Dinanath Soni
Executive Director
Si2 Microsystems Pvt Ltd

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Former Chairman of DRDO, Govt. of India
(Presently Professor of Practice, Dept. of EE, IIT Madras)

S. Christopher
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Former **Seceretary**, Department of Defence R &D and **Chairman DRDO**, MoD, Government of India

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Silicon Photonics Team

CoE-CPPICS-IIT Madras.

I am delighted to congratulate 'Team Silicon Photonics', on the occasion of the inauguration of our "Center of Excellence at Center of Programmable Photonics Integrated Circuits and Systems". I am equally proud of being part of the team.

The efforts on the design development of Programmable Photonic Integrated Circuits and Systems had steadfast progress right from the bringing and achieved several path breaking successes enroute. This is yet feather in the cap and another major mile stones in the journey of Silicon Photonics Team, which is rightfully recognized by the government of India.

I take this opportunity to once again congratulate my friends and team mates, on this remarkable journey and wish many more successes in this extraordinary journey!

S Christopher

Chief Investigator of CNNP, IIT Madras

Enakshi Bhattacharya, PhD
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16th October, 2023

Congratulations and the very best wishes to Professor Bijoy K. Das and his team on the inauguration of the Centre for Programmable Photonic Integrated Circuits and Systems (CPPICS), a centre of excellence (CoE) initiative by the Ministry of Electronics and Information Technology (MeitY), Government of India. The silicon photonics program at IIT Madras, one of the earliest in India, has reached this stage by sheer grit, hard work and innovation from the CPPICS team. Starting with materials, waveguides, resonators and interferometers the group is already at the stage of fabricating photonic ICs now and can hold its own when compared to any such program globally.

Being one of the PIs of the Centre of NEMS and Nanophotonics (CNNP), also funded by the MeitY in 2011, this brings added happiness in seeing a tree grow from the seeds germinated then. Now that the tree is mature, we expect it to bear flowers and fruits that can be beneficial across a myriad of applications, be it communications or quantum computing.

Wishing the CPPICS all success in its mission.

Sincerely,

E. Bhattacharya

Chief Investigator of CNNP, IIT Madras

Dr. Nandita DasGupta
Professor

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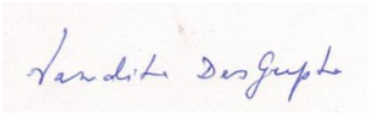
First of all, I would like to congratulate Professor Bijoy K Das and his team on the inauguration of the Centre of Programmable Photonic Integrated Circuits and Systems (CPPICS), which is a Centre of Excellence funded by The Ministry of Electronics and Information Technology (MeitY), Government of India. I have seen the research activity in the area of silicon photonics at IIT Madras grow from strength to strength in the last fifteen years under the able guidance of Prof. Das. Starting from the fabrication of basic optical components like waveguides, the CPPICS team is now capable of fabricating optical ICs. The infrastructure created by Prof. Das and his team is not just one of the best in India, it is also at par with leading international groups.

MeitY has already supported silicon photonics activity at IIT Madras generously through the projects titled Centre of NEMS and Nanophotonics (CNNP) and Nanoelectronics NETwork for Research and Applications (NNetrA) for which I am one of the two PIs. With the inauguration of CPPICS, I expect the research group to scale newer heights in the years to come and wish them great success.

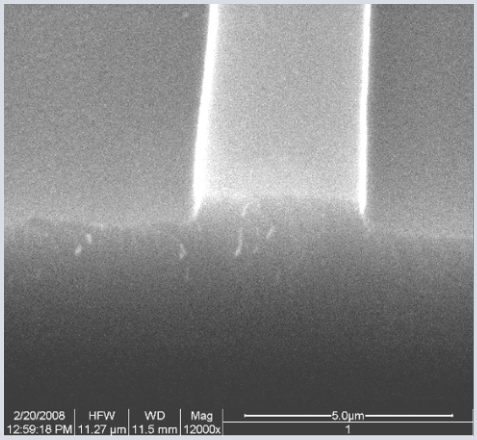


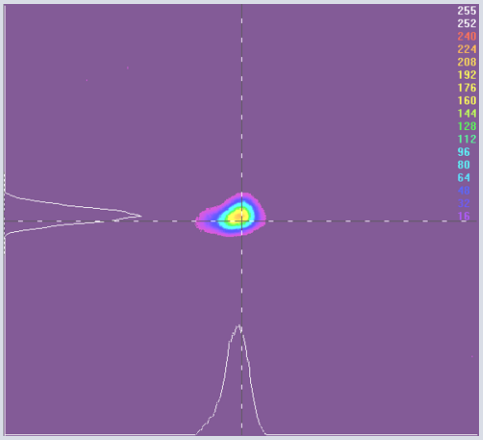
Silicon Photonics @ IIT Madras
Journey from IOLab to Silicon Photonics CoE-CPPICS
(Aug. 2006 - Dec. 2020)

Though the interests in silicon photonics research among Indian scientists and engineers were noticeable here and there, no planned long-term research goals were set until IIT Madras took the lead to start a silicon photonics research group in 2006. Since then the group at IIT Madras has been actively engaged in novel design, fabrication and characterizations of silicon photonic devices for communication systems and sensor applications. By the end of 2011, various prototype devices were demonstrated by making use of conventional i-line lithography technology (1-μm node) available at IIT Madras. With the availability of nanofabrication facilities at the Centre for NEMS and Nanophotonics (funded by MeitY Govt. of India), the research program was raised to the next higher level – research outcomes have been presented in international conferences, published in peer reviewed journals, and filed as patents as well. The goal of the research group is now set to carry out world class silicon photonics research encompassing novel device designs, CMOS compatible fabrication process optimizations and experimental demonstrations leading towards cost-effective, multi purpose programmable photonic processor chips for microwave and quantum photonic engineering applications. The *Silicon Photonics CoE-CPPICS* is the latest addition in our timeline. Some landmark glimpses of our journey are highlighted below.

Landmark 2007: The first silicon photonic device characterization setup was developed jointly by our first MS Research Scholar Rupesh Navalakhe (jointly guided by Prof. Nandita DasGupta) and first PhD Research Scholar Shantanu Pal in the OCEAN Lab. The optical bench was placed on the top of a coconut coir bed for vibration isolation. All the components used to build this setup was collected from the storage (left over from Prof. Raina) except the IR CCD camera on the extreme right which was bought from the seed grant of Rs. 5 Lakhs from IIT Madras.

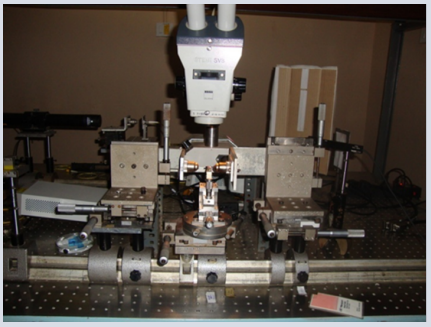
Landmark 2008: The first single-mode waveguide was fabricated at the Microelectronics & MEMS Lab using silicon-on-insulator (SOI) substrate with a device layer thickness of 5 μm. The guided mode was captured by the IR CCD camera which is also shown here.



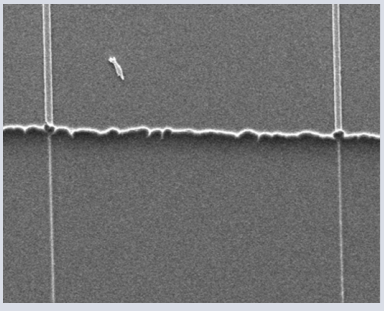


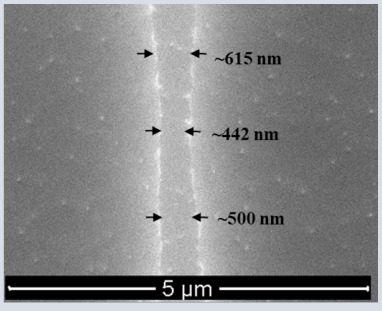
Landmark 2009: The number of students and research scholars increased to a team of eleven and we started calling it as the Integrated Optoelectronics Group. The Integrated Optoelectronics Lab was built in Room No. CSD106.

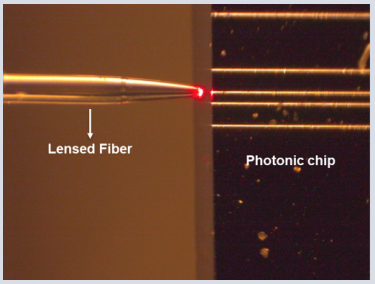
Landmark 2011: Some working silicon photonic prototype devices fabricated at IIT Madras were fiber-pigtailed and packaged in SAMEER, Mumbai. The project was funded by the Department of Information Technology (DIT), Govt. of India.

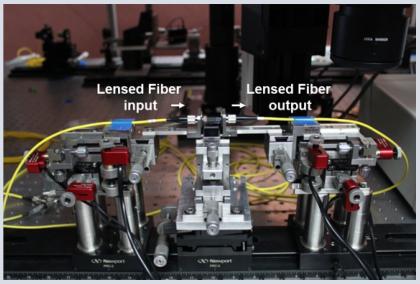


Landmark 2012: When the whole world was progressing fast in the area of silicon photonics technology by taking advantage of their advanced nano fabrication facilities, our PhD research scholar Sujith Chandran was trying desperately to demonstrate photonic wire waveguide using age-old microelectronics fabrication facilities at IIT Madras. However, his efforts finally led to the filing of a US patent, which was granted at a later date.

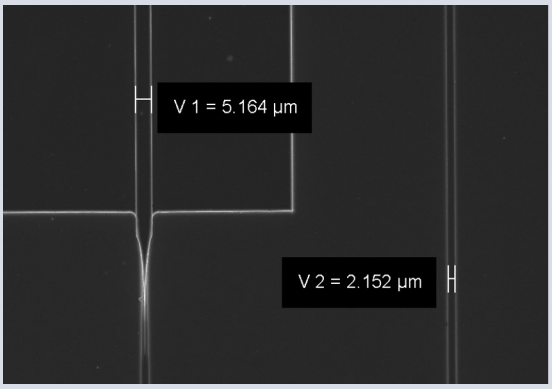


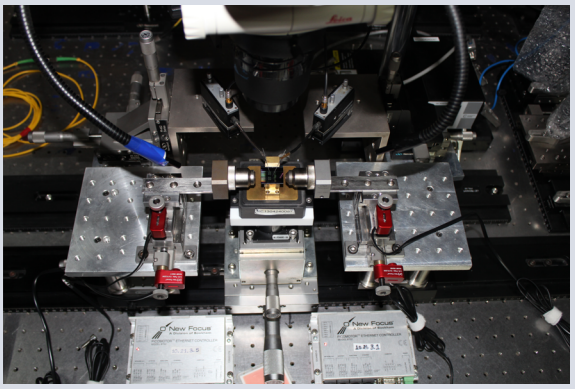




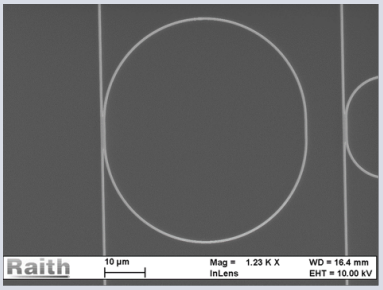


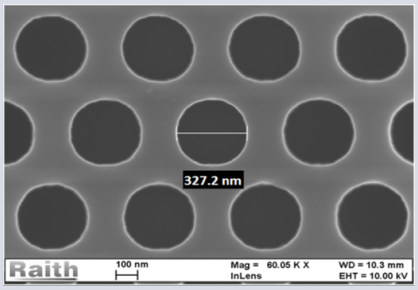
Landmark 2012: Finally, the Centre for NEMS and Nanophotonics (CNNP) was funded by the Department of Electronics and Information technology (DeitY), Govt. of India and our silicon photonics technology started evolving very fast by the hard works of a dedicated team of research scholars led by Sujith Chandran and P. Sakthivel.



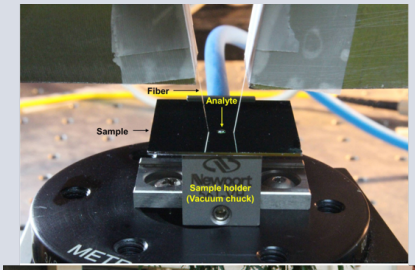


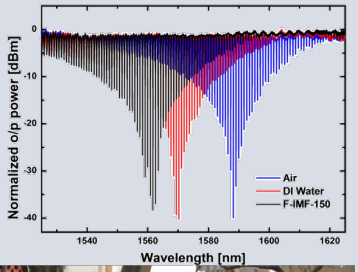
Landmark 2015: The first photonic wire waveguide based microring resonators (MRRs) and photonics crystal structures were demonstrated in silicon-on-insulator (SOI) with device layer thickness of 220 nm (CMOS photonics foundry compatible) using CNNP facilities.





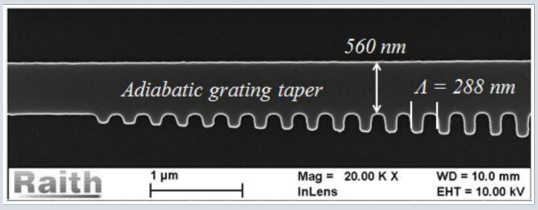
Landmark 2017: A specially designed microring resonator was fabricated to demonstrate evanescent field induced refractive indexing sensing purpose. This was the first silicon photonic wire waveguide device used for lab-on chip sensing application using fiber-optic grating coupling setup in our Integrated Optoelectronics Lab (now moved into CSD108).



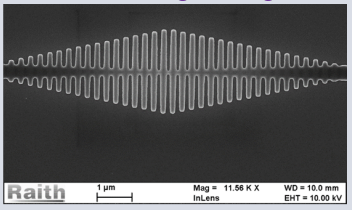


Landmark 2019: Almost all the CMOS fabrication process compatible silicon photonic basic building blocks were demonstrated using in-house fabrication facilities; some of them are with novel design architectures and can be directly used for programmable photonic integrated circuits.

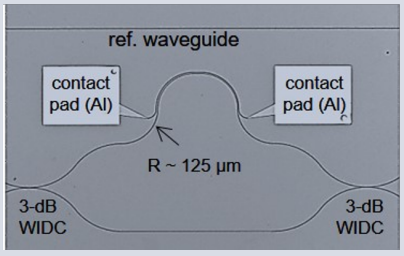
Distributed Bragg Gratings



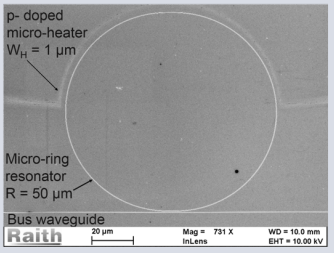
Sub-Wavelength Gratings



Mach-Zehnder Interferometer with Metal Heater



Microring Resonator with Doped Heater



Landmark 2020: The Silicon Photonics Centre of Excellence - Centre for Programmable Photonic Integrated Circuits Systems (Silicon Photonics CoE-CPPICS) was proposed with an ambitious list of objectives. It was granted on 29th December 2020 and in midst of Covid'19 Pandemic, the team CoE-CPPICS started working on programmable silicon photonic processors following product research and manufacturing model.

Centre at a Glance

The Centre for Programmable Photonic Integrated Circuits and Systems (CPPICS) is one of the centre of excellence (CoE) initiatives by the Ministry of Electronics and Information Technology (MeitY), Govt. of India. It is hosted by the Department of Electrical Engineering, IIT Madras with a long-term mission for catering R&D in the area of programmable photonic integrated circuits and systems using CMOS compatible silicon photonics technology for solving various levels of complex problems.

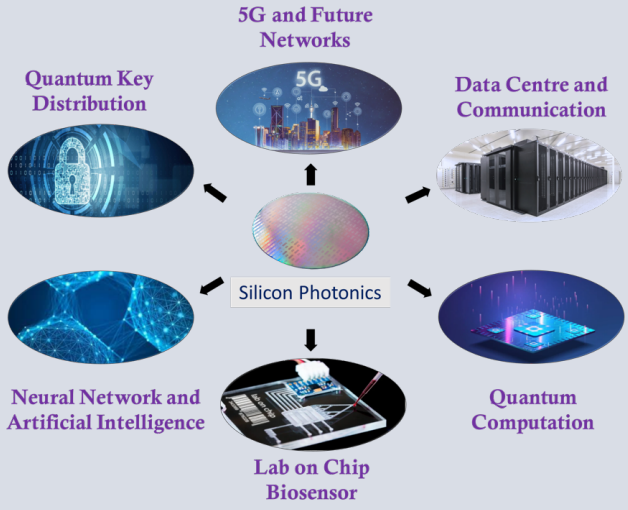
Background and Funding Status

The CoE-CPPICS has been established on 1st January 2021 in the Department of Electrical Engineering, IIT Madras with a substantial seed funding of Rs. 2,665 Lakhs (USD 3.5M) from the MeitY, Govt. of India, (Sanction No. GG-11/15/2020/EMCD, dated 29.12.2020), in-kind contribution of Rs. 325 Lakhs (USD 0.5M) from the Si2 Microsystems Bangalore and subsequent additional funding of Rs 425 Lakhs (USD 0.7M) from IIT Madras. This recognition and funding has been possible because of 17 years (since 2006) of R&D work by the Integrated Optoelectronic Research Group led by Prof. Bijoy Krishna Das in the area of silicon photonics technology.

Mission

Our mission is to build capacity in all verticals of silicon photonic integrated circuits manufacturing eco-system through focused R&D and nurture Indian photonics industry for immediate needs in domestic and international markets.

Current Research Activities



The immediate focus of this CoE is to provide better solutions for microwave and quantum photonics applications such as advanced photonic processors to be used in high-performance RF transceivers, scalable linear optical quantum computing processors for the next-generation qubit computation, and chip-level quantum key generation and distribution circuits, etc. CPPICS is actively developing indigenous PIC design rules and hardware infrastructure for precision packaging for system-level applications.

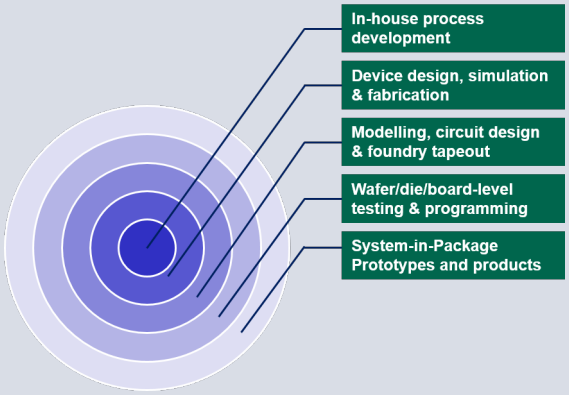
Quantum Information Processing

- Quantum Random Number Generation
- Quantum Key Distribution
- Quantum Sampling Algorithm

Microwave Photonics

- Programmable Radio Frequency Filter
- Optoelectronic Oscillator
- Photonic Beamforming

In our unwavering commitment to driving innovation and fostering technological advancements, we, at the Center of Excellence, are actively engaged in pioneering research starting from technology development to packaging solutions. Our expertise spans a diverse spectrum of domains, with esteemed faculty members from IIT Madras playing an integral role. Their invaluable guidance and expertise are essential to our research endeavors.



Our Experts

Chief Investigator

Prof. Bijoy Krishna Das

The center is being led by Chief Investigator Prof. Bijoy Krishna Das, steering CPPICS toward excellence in research and innovation. Since August 2006, his dedicated efforts have been instrumental in spearheading the development of in-house silicon photonics device technology at IIT Madras.

Chief Technology Officer

Mr. Arnab Goswami

Arnab Goswami joined as the Chief Technology Officer (CTO) of the centre in January 2022. He has been involved in the overall lab infrastructure development, fabrication process development, supervising design and foundry tape-outs. He is also responsible for the creation and execution of self sustenance plan and techno-commercial roadmaping.

Co-Investigators

Prof. Enakshi Bhattacharya
MEMS & Photonics

Prof. Amitava DasGupta
Device Modelling & VLSI

Prof. Nandita DasGupta
Microelectronics & Photonics

Prof. Anil Prabhakar
Quantum Photonics

Prof. Anjan Chakravorty
Compact Modelling

Prof. Deleep R. Nair
Design, Fab and Testing

Prof. Deepa Venkitesh
Fiber Optics & RF Photonics

Prof. Janaki Viraraghavan
Digital IC Design

Prof. Sankaran Aniruddhan
Analog IC design

Prof. Sudharsanan S
Photonics Technology

Prof. Sargunaraj Christopher
Microwave Engineering

Industry Advisory Board

Chairman

As the chairman of CPPICS Industry Advisory Board, I am committed to coordinate with other board members to provide guidance to the team CoE-CPPICS to continue its activities following the Product Research Development and Manufacturing model.

Dr. Mallik Tatipamula
CTO at Ericsson
San Jose, California, USA

Members

Dr. Vivek Raghunathan
Founder & CTO
Xscape Photonics Inc., USA

Dr. Prith Banerjee
CTO, Ansys Inc.
Palo Alto, California, USA

Mr. Arjun Kumar Kantimahanti
Senior Vice President
SilTerra, Malaysia

Mr. Kailash Narayanan
President & General Manager
Keysight Technologies, USA

Mr. Vijay Janapaty
Vice President & General Manager
Broadcom Inc., USA

Mr. Vikas Gupta
Senior Director
GlobalFoundries USA

Dr. Ravi M. Bhatkal
Managing Director
India Element Solutions Inc, India

Mr. Dinanath Soni
Executive Director
Si2 Micro System, India

Dr. Steve Johnston
Vice President
Merck KGaA Darmstadt, Germany

Mr. Narayan Srinivasa
Director
Intel Corporation USA

Dr. Kishore Kamath
Vice President
R&D, Intel Corporation USA

Team Members

Postdoctoral Researchers

Diptasree Maitra Ghosh
SOI & SiN Technology Development

Nagarajan Nallusamy
Non-Linear Photonics & PIC Packaging

Shamsul Hassan
PIC Packaging & QRNG

Goutham Ezhilarasu
PIC-EIC Packaging

PhD Scholars

Suvarna Parvathy
High-Speed Modulator

Ram Mohan Rao Boyapati
Quantum Key Distribution

Ashitosh Velamuri
Microwave Photonics & Compact Modeling

Anushka Tiwari
SiN Technology Development & Optoelectronic Oscillator

Pawan Kumar Pandit
High Speed Photodetector & Feedback Control

Riddhi Goswami
SiN Technology Development

Ankan Gayen
QRNG & PIC Packaging

Kumar Piyush
Programmable Photonics & EIC-PIC Co-Integration

Yash Raj
Programmable Photonics & Boson Sampling

Anjana James
Compact Modeling & PDK Development

Dibyanchal Sahu
EIC-PIC Integration

Mayukh Mandal
Integrated Quantum Photonics

MS(Res.)/M.Tech Scholars

Pratyasha Priyadarshini
Distributed Bragg Reflector based Filters

Pranita Kumari Swain
SiN Technology Development
Non-Linear Photonics

Shruti Pandey
Compact Modeling & PDK Development

Lokesh Bhaskar Gajbhiye
EIC-PIC Integration

Project Staffs

Vinoth S.
PIC Packaging

Sarad Subhra Bhakat
Si-SiN Hybrid Integration & SiN Technology Development

Akash Shekhar
EIC-PIC Integration

Administrative Secretary

B.Sindhura

Logistics Secretary

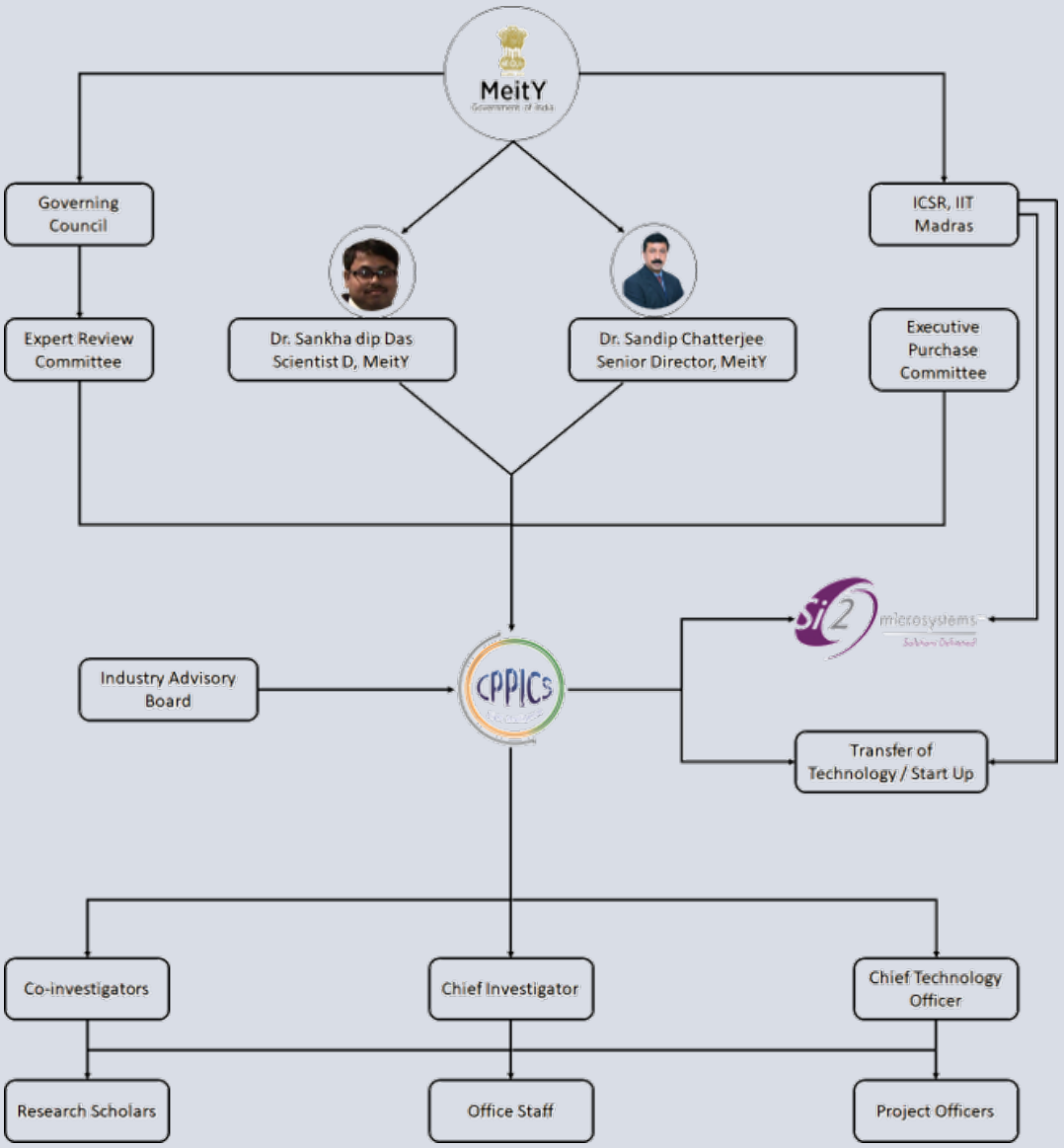
G.Inbasekaran

Lab Assistant

M.Mohan Babu

Organizational Structure

This CoE Organization is composed of a Governing Council featuring esteemed members, an Expert Review Committee with exceptional expertise in similar and versatile research areas, Principal and Co-Investigators representing the renowned institution IIT Madras, ICSR – IIT Madras, a Chief Technology Officer, Academic and Industry veterans as collaborators, dedicated and proficient research scholars, dynamic Project Officers, and skilled office staffs.



Reserach Labs and Facilities

In January 2021, our team embarked on an ambitious and exciting journey to transform an ordinary laboratory space into a cutting-edge design and characterization facility. In April 2021, the administration IIT Madras approved the allocation of laboratory space for our centre of excellence. Progressing swiftly, the construction and renovation phase were in full swing by the conclusion of 2021. All the major equipment have been installed and lab is now in completely operational mode.

Exp. lab space given to CPPICS

Exp. lab under construction

Exp. lab after construction

Reserach scholars during experiments

Reserach scholars in fabrication process lab

In addition to CPPICS's own facilities, we have in-house fabrication facilities at Center for NEMS and Nanophotonics (CNNP), IIT Madras. The cleanroom within CNNP spans over 2500 square feet and is equipped with state-of-the-art systems for deposition, lithography, etching, and characterization. This robust infrastructure enables us to conduct cutting-edge research and development while maintaining high standards of precision and quality.

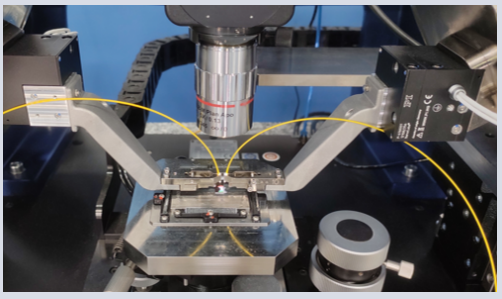
- Electron-Beam Lithography
- DUV and i-line Lithography Systems
- Laser Mask Writer
- LPCVD and PECVD Systems
- Chemical Mechanical Polishing
- Oxidation and Diffusion Furnaces

Major Process facilities

Major Characterization Equipment

- 8 channel superconducting Nanowire Single-Photon Detector System
- Lightwave Component Analyzer and Vector Network Analyzer (26.5GHz & 50 GHz)
- High-Resolution Optical Spectrum Analyzer(Resolution Bandwidth 0.04 pm)
- Real-time Digital Oscilloscope (50 GHz)
- Arbitrary Waveform Generator (50 GHz)
- Wafer-scale silicon photonics probe station

Cleanroom facilities at CNNP



Wafer-scale silicon photonic probe station

State-of-the-Art R&D Activities

At CoE-CPPICS, we engage in product research development and manufacturing model to build the complete ecosystem for the photonic integrated circuits starting from device design to prototype development and field tests, in India. Our work encompasses device design, compact modeling, development of waveguide technology in SOI, SiN, and SOI/SiN hybrid platforms. We specialize in the development of optimization techniques for a programmable photonic circuits for the applications in the field of microwave photonics, quantum photonics and computation. Additionally, we are also deeply engaged in photonic system integration, with a keen focus on electronic-photonic integration, fiber optic attachment and packaging.

Device Design and Compact Modelling

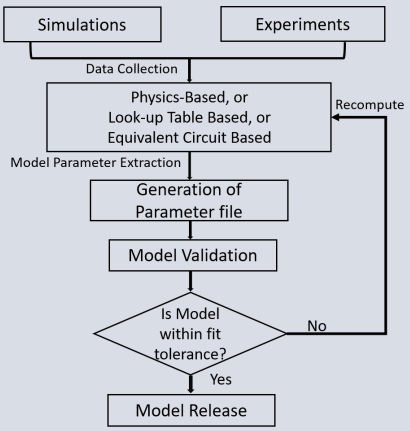
In the process of scaling photonic circuits, an in-depth exploration of fundamental photonic devices is of paramount significance. The development of compact models for these devices is a pivotal step, enabling photonic designers to create process design kits (PDKs). These PDKs derived from the foundries, empower end-users to efficiently design the specific devices they require.

Compact Modelling of Silicon Photonic Devices

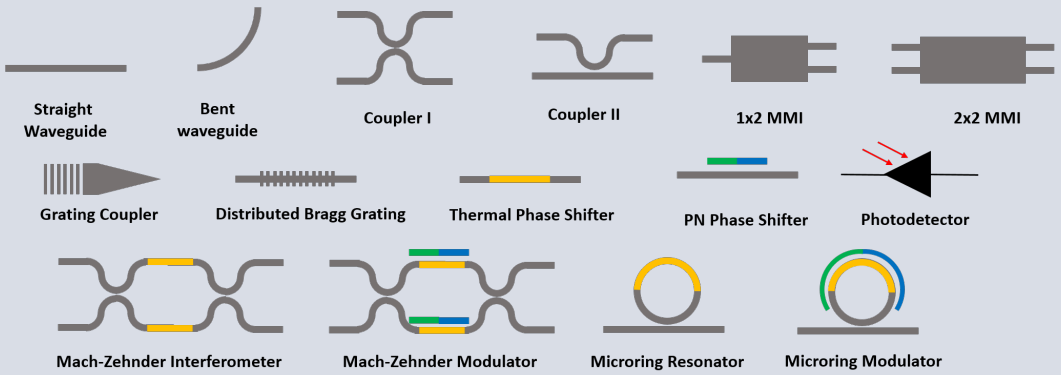
Associated Reserach Scholars: *Shruti Pandey, Anjana James, Ashitosh Velamuri, Nagarajan Nallusamy, Shamsul Hassan, Suvarna Parvathy, Pawan Kumar*

The ever-increasing demand for bandwidth in telecommunications has enabled the growth of optical data transmissions over the last two decades. Owing to the high demand, the integration density of the photonic integrated circuits is growing in a similar trend to electronic circuits. Even though component level models of photonic devices are very well established, integration of such models in to circuit simulations are very rarely found and are very crucial to design and analyze the optical link.

Compact models of circuit elements are mathematical models based on simulation and experimental results that are simple and accurate to be incorporated in circuit simulators. Compact models can also provide fabrication tolerance. Devices compact modeling can be done in three ways depending upon the feasibility of modeling; it can be either device physics based model or just a look-up table based model or could even be an equivalent circuit representation which can be easily simulated in any circuit simulator.

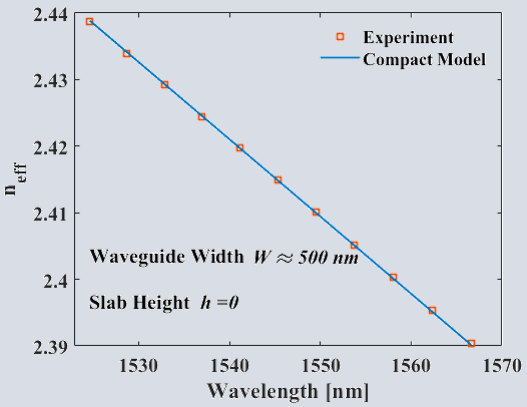


Here at CoE-CPPICS, we have recently started working towards the development of compact models of all the necessary active and passive photonic devices (modulators, photodetectors, waveguides, couplers, gratings, interferometers, resonators and phase shifters) that are required for the analysis of a large scale photonic circuit in a electronic/photonic circuit simulators. Our aim is to develop simple yet powerful models, giving the large degree of freedom to the design engineers in terms of various geometrical and operational parameters of the components.

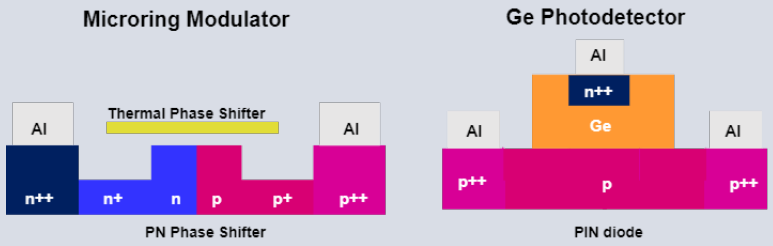


Basic passive and active discrete photonic components of a large scale photonic integrated circuit.

The compact modeling of the photonic integrated circuit poses the unique challenge of culminating the well established frequency-domain models of passive structures and the time-domain models of the active structures. To develop the mentioned compact model library for the discrete photonic components, an accurate model to estimate the waveguide effective index is very important. A look table based approach was followed for the effective index modeling over the range of geometrical and operational parameters of the waveguide. The developed waveguide compact model has been validated with the fabricated devices, resulting in the accuracy of $\sim 10^{-3}$, which is within the limit of fabrication tolerance.



Validation of the effective index model with the experimentally extracted data



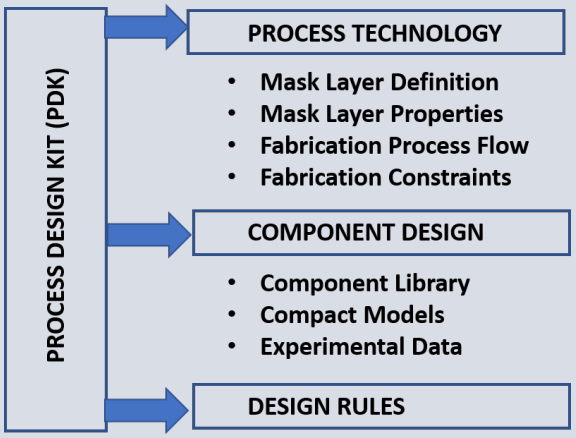
Cross-sectional view of microring modulator and heterogeneously integrated Ge photodetector on SOI platform.

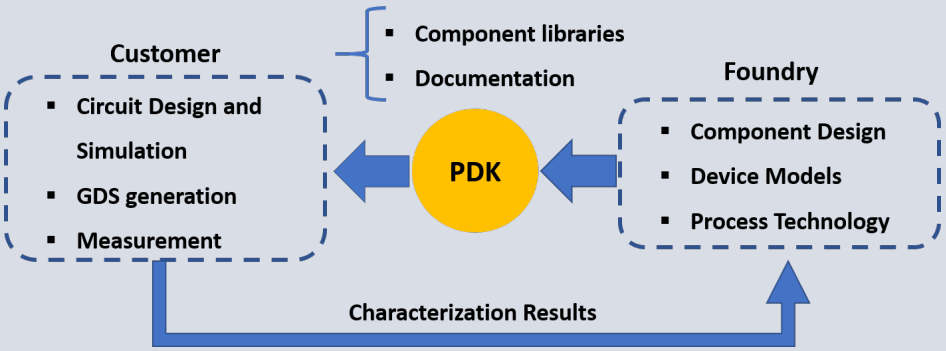
We are currently working towards the extension of the waveguide compact model to other complex photonic devices like couplers, PN phase shifters, thermal phase shifters, modulators, PIN diodes and photo detectors. We also look forward to realise electronic photonic co-simulation using electronic design automation tools to simulate large scale electro-optic circuit for applications like LIDAR, neuro-morphic computing and quantum computing.

Process Design Kit Development

Associated Research Scholars: *Arnab Goswami, Pawan Kumar, Ashitosh Velamuri, Kumar Piyush, Ram Mohan, Suvarna Parvathy*

A Process Design Kit (PDK) is a compilation of information about photonic devices which can be used for circuit design and fabrication. PDK contains information about the process technology, component design and design rule checks for the designer to come up with an optimal foundry compatible design. The information related to process technology contains the fabrication process flow, mask layer information, mask layer properties and the fabrication constraints for the specific foundry. PDK has a library of basic photonic components, their compact models and experimental testing data for the designer to make optimal design choices. In addition, PDK provides a set of design rule checks depending on the process technology of the foundry.

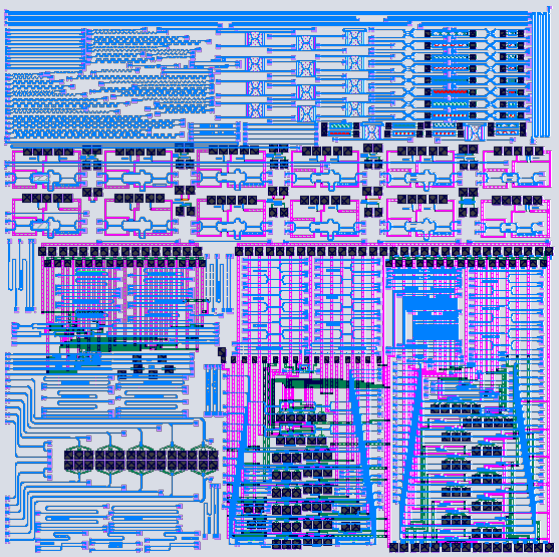




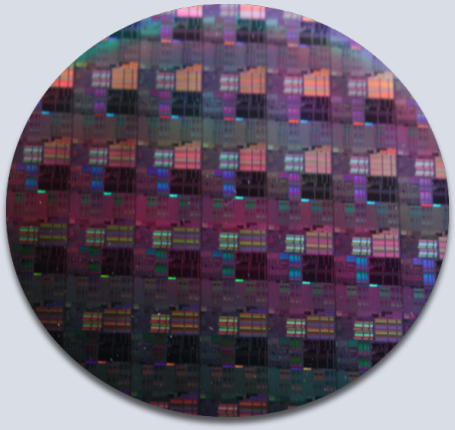
PDK serves as a link between the circuit designer and the foundry enabling the circuit designer to design photonic circuits using the different components available in the component library. The component library is in the form of analytical or physics based models for the basic passive (waveguides, waveguide bends, power splitters, grating couplers) and active (modulator, photodetector) photonic devices. Based on these available component libraries, the customer designs the GDS layout and submits the design to the foundry for fabrication. For large scale photonic circuit design, there can be PDKs that offer photonic circuit simulator compatible blocks which will enable the designer to evaluate the circuit performance well before the actual fabrication. The layout of the desired circuit is shared with the foundry, following which mask preperation and fabrication is carried out. Based on the characterisation results of the fabricated devices, required updates are made to the existing PDK.

SilTerra joins hands with CPPICS

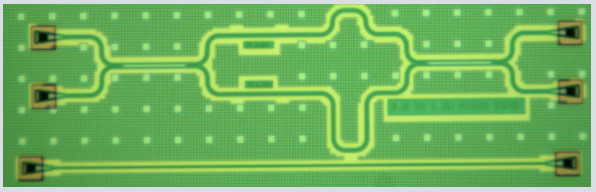
One of the leading global semiconductor foundries, SilTerra, Malaysia has joined hands with CPPICS to develop silicon photonics PDK. For our first run of tape out, our scholars have designed different passive components which includes waveguides, waveguide bends, power splitters, wavelength filters and Mach Zehnder Interferometers. The structures given for tape out have been fabricated by SilTerra and the optical characterisation of the fabricated devices are actively being carried out at CPPICS. These characterisation results will be modeled to form our first-cut PDK for SilTerra. This run will be followed by active device fabrication, characterisation and modeling. We are also looking forward to developing models for devices like distributed Bragg reflectors (DBR), waveguide crossings and microring based filters which are not available currently in any other existing foundry PDK.



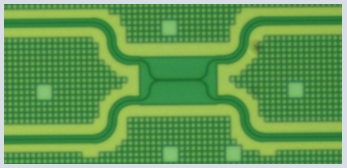
Layout design of various active and passive devices on 8 mm × 8 mm chip, for tape-out from SilTerra



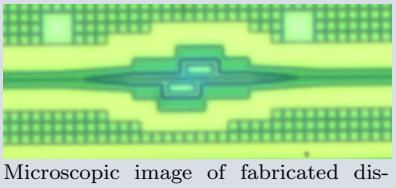
8 inch wafer fabricated at SilTerra, Malaysia



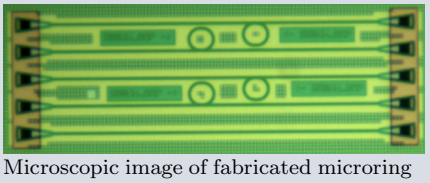
Microscopic image of fabricated unbalanced MZI with reference waveguide



Microscopic image of fabricated directional coupler



Microscopic image of fabricated distributed Bragg reflector



Microscopic image of fabricated microring resonator with grating couplers

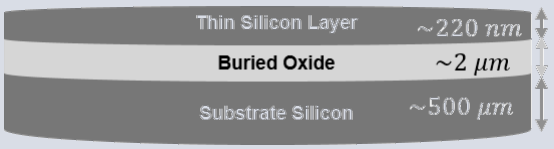
Fabrication Process Development

We at CoE-CPPICS are working in two different technology platforms i.e. Silicon on Insulator (SOI) and Silicon Nitride on Insulator (SNOI). Over the past 15 years, we have achieved a high level of maturity in SOI waveguide technology processes. This advancement has allowed us to demonstrate various innovative passive devices, circuits, and phase shifters for multiple applications maintaing a waveguide loss of less than 5 dB/cm. For the past 2 years, we have been involved in developing in-house SNOI waveguide technology process starting from bare silicon wafer, growing silicon di-oxide on it, followed by LPCVD silicon nitride deposition. Very recently, we have achieved the low loss waveguide with propagation loss below 1 dB/cm. To further reduce the loss we are working constantly to refine our fabrication process steps and have also started working on damascene process. Furthermore, we are also actively working towards the hybrid integration of Si and SiN to demonstrate efficient circuits in terms of lower loss and thermal budget.

SOI Waveguide Technology

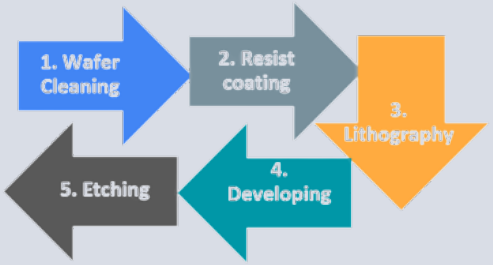
Associated Reserach Scholars: *Suvarna Parvathy, Ram Mohan, Arnab Goswami, Ashitosh Velamuri, Ankan Gayen, Kumar Piyush, Pawan Kumar, Yash Raj*

SOI wafers consist of a thin layer of silicon (the device layer), buried oxide and silicon substrate stacked one above another as shown below. The thin silicon layer is used to fabricate waveguides and other passive or active optical devices. The buried oxide prevents propagation of light into the silicon substrate thereby supporting optical modes in tne device layer guided by total internal reflection.



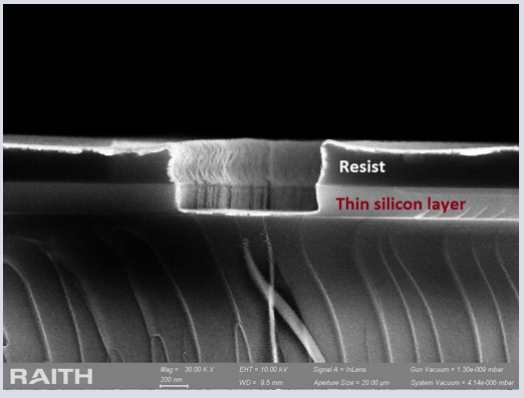
SOI wafer

Fabrication flow of optical devices on SOI includes several process steps. We have shown the major steps here. First, we start with cleaning of SOI wafer which includes standard organic cleaning to remove oils followed by inorganic cleaning to remove metallic oxides. After cleaning we need to dehydrate the wafer to remove any water content. Now, we can go for resist(positive/negative) coating. Afterwards on this coated sample, pattern is transferred from mask either using E-beam lithography or photo-lithography.



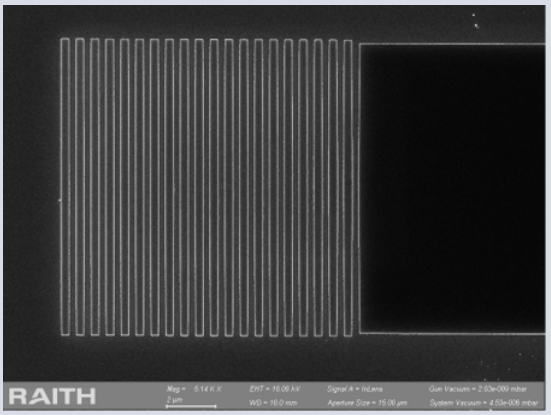
SOI process flow

Once, the pattern is transferred, this wafer is put into developer solution to remove the exposed/unexposed resist (depending on resist type). After developing we go for etching to get our final devices (passive).

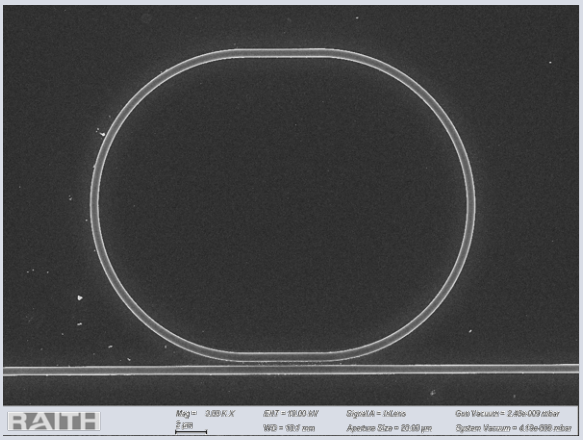


SEM cross-section view of etched device on SOI

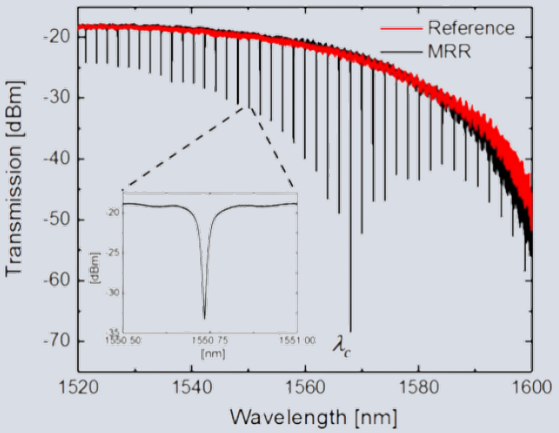
The core research of our group involves novel device designs, CMOS compatible fabrication process optimizations and subsequent experimental demonstrations leading towards cost-effective, energy-eficient and high-speed silicon photonic circuits for various applications. As of now, various prototype and packaged devices like power splitters, channel interleavers, variable optical attenuators, p-i-n phase shifters/modulators, ring resonators, DBR (Distributed Bragg Reflector) and SWG (Sub-Wavelength Grating) filters etc., have been demonstrated by utilizing the resources at our centre of excellence CPPICS and nanofabrication facilities at IIT Madras.



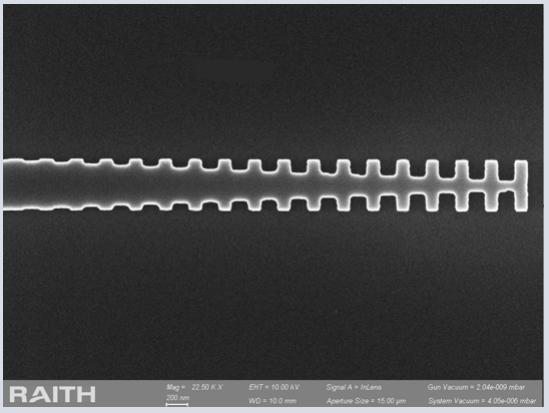
SEM top view of grating coupler on SOI



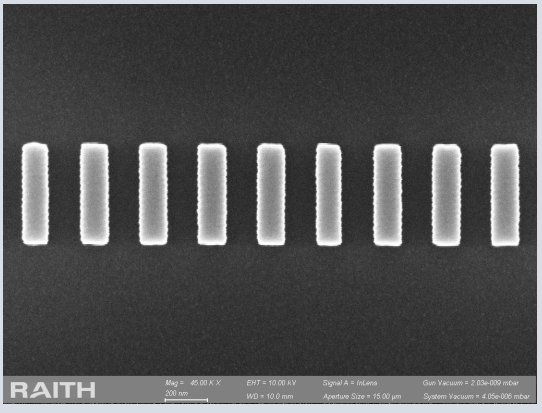
SEM top view of a Micro Ring Resonator on SOI



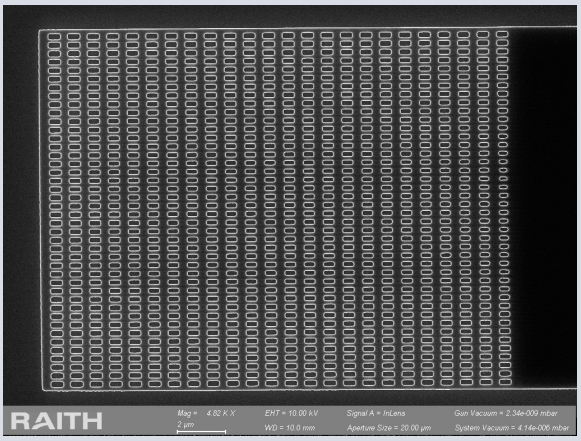
Measured transmission characteristics of a Micro Ring Resonator along with a reference waveguide



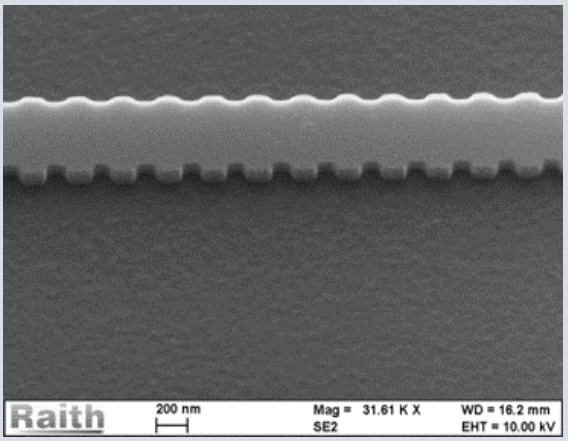
SEM top view of SWG Taper on SOI



SEM top view of SWG waveguide on SOI

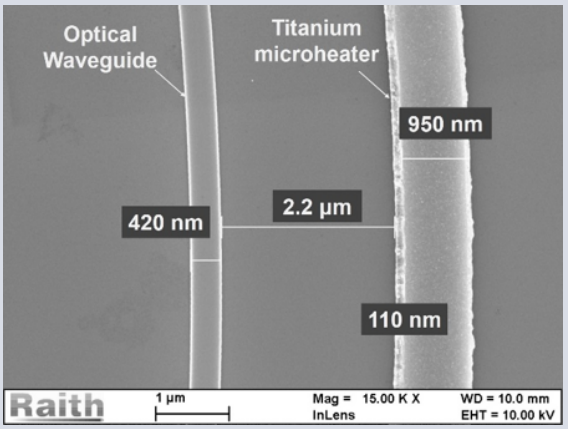


SEM top view of 2-D grating on SOI

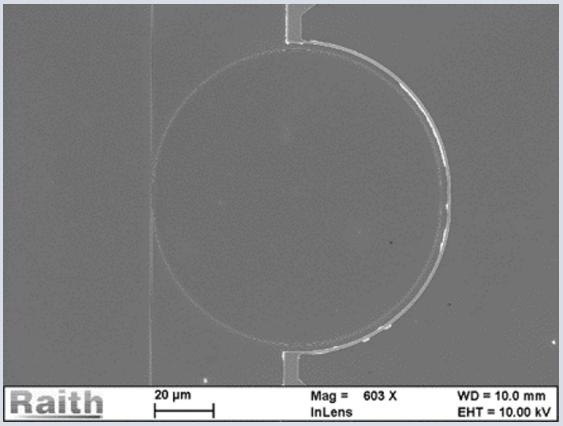


SEM angled view of DBR on SOI

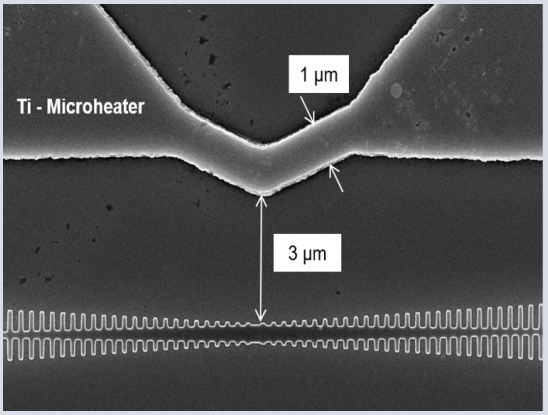
To address the fabrication imperfections and to operate these devices at specific working points or to switch between different states, active control is essential. One way is to use thermo-optic modulation by placing micro-heaters either at the side or on top of the waveguides and using heating to change the refractive index. Fabrication of these heaters start once the passive devices are patterned.Since positioning of the heaters demand high precision, we use E-beam lithography. Aluminium (Al) is used for contact padS and Titanium (Ti) for metal heater fabrication. Below we have shown a MicroRing Resonator (MRR) of $50\mu m$ ring radius with side Titanium (Ti) side heater.



SEM zoomed-in view of MRR with side heater



SEM top view of MRR with side heater

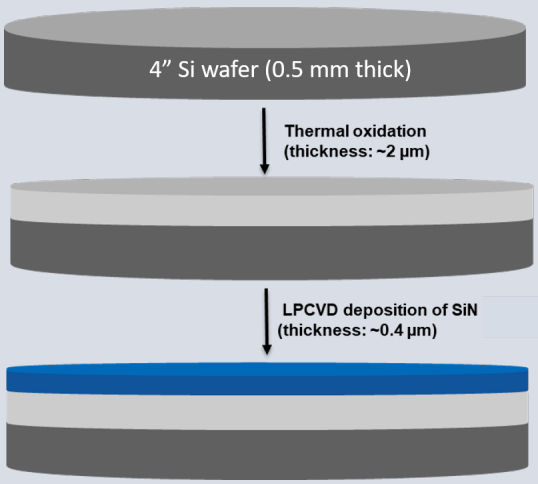


SEM zoomed view of DBR cavity with side heater

SiN Waveguide Technology

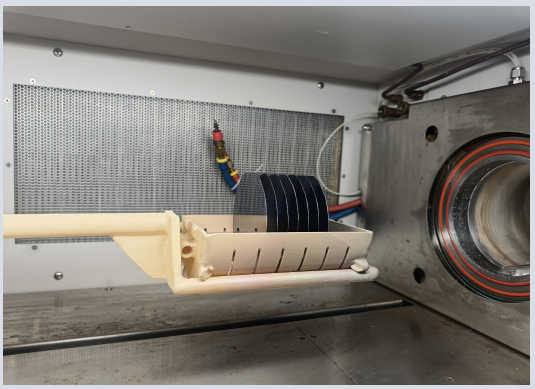
Associated Reserach Scholars: *Riddhi Goswami, Pranita Ku. Swain, Anushka Tiwari, Sarad S. Bhakat*

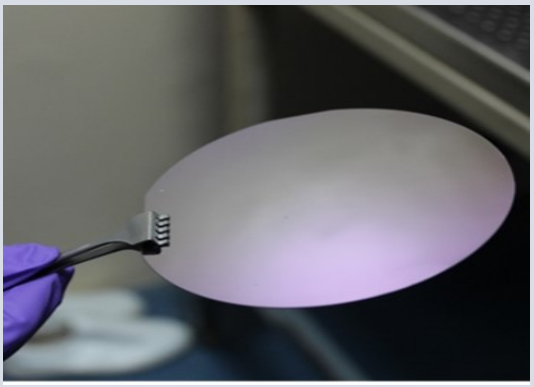
In addition to Si core, SiN (Silicon Nitride) is gaining major attention due to its relatively lower waveguide losses, wider transparency and less sensitivity to temperature fluctuations and fabrication variations. The growth of an optical grade oxide layer (for bottom cladding) and subsequent deposition of SiN device layer are the most important aspects for the realization of large-scale photonic integrated circuits with acceptable waveguide losses and fabrication yields. Our group has been working towards fulfilling that goal and has made conceivable achievements so far.We are able to grow good quality thermal oxide wafers($\approx 2\mu m$) and stoichiometric, crack-free SiN wafers($\approx 0.4\mu m$) with excellent wafer scale variations.



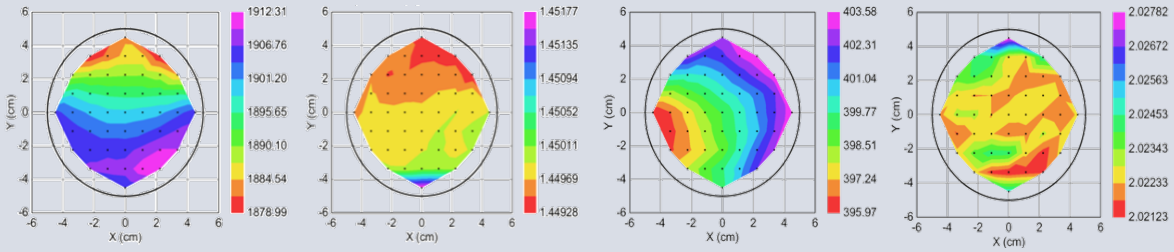
SiN Deposition Process Flow

We have also been able to demonstrate losses below 1 dB/cm and 3 dB/cm in LPCVD (Low Pressure Chemical Vapour Deposition) and PECVD (Plasma Enhanced Chemical Vapour Deposition) SiN platforms (both on $2\mu m$ thermal oxide) respectively using traditional waveguide technolgy like the SOI process which involves patterning on device layer. Both the platforms were developed completely indigenously here at IITM starting only with 4 inch bare Si wafer.


Loading of thermal wafers in SiN furnace


In-house fabricated SiN wafer

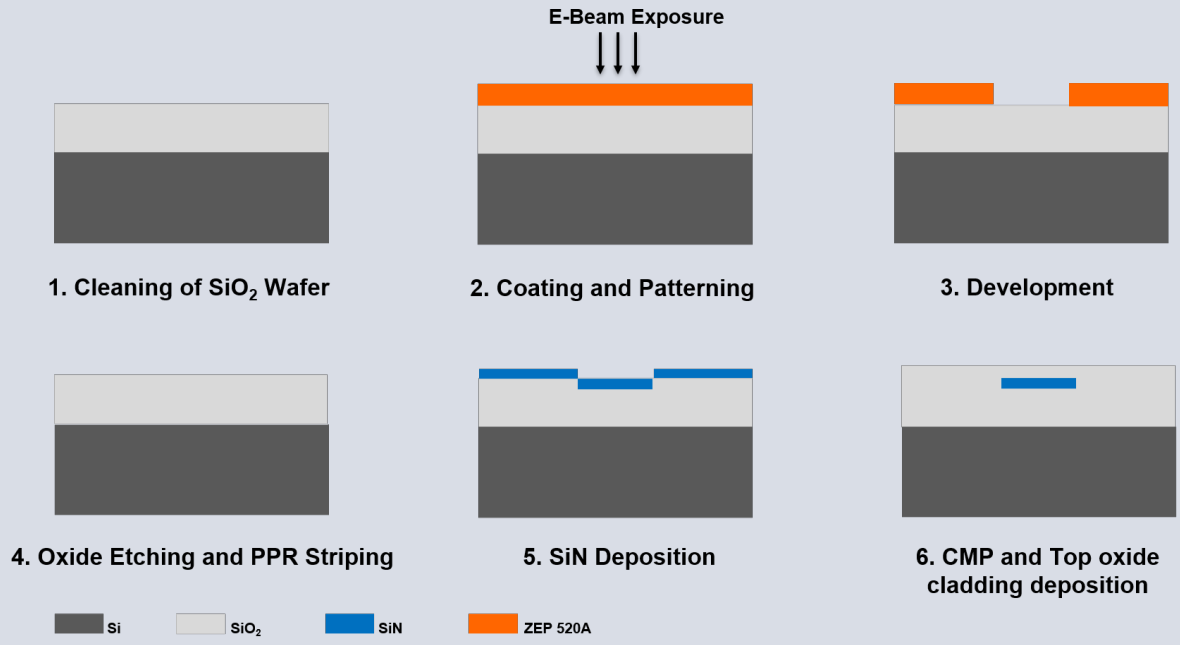
Although LPCVD SiN provides low-loss waveguides, the thickness is limited to 400 nm due to tensile stress within the film. However in order to harness the nonlinear properties of SiN, we need relatively



SiO_2 SiN

Wafer scale ellipsometric measurements showing thickness and refractive index variations(1550 nm) respectively

thicker films for demonstrating applications such as frequency comb generation. At CoE-CPPICS, therefore we are currently trying to establish a process flow for Damascene which can provide eficient stress control and prevent the film cracks (for higher thickness SiN, >400 nm). The process is based on first etching trenches into buried oxide (BOX) layer and then filling the trenches with SiN for waveguide core and finally planarising the surface with Chemical Mechanical Polishing (CMP). A top oxide layer may be deposited later depending on requirements. Damascene is expected to give lesser waveguide losses since we are not directly etching the SiN device layer leading to improved side-wall roughness. Low loss, planar optical waveguides have the potential to be a key enabling technology for a wide range of applications, such as delay lines, ultra narrow linewidth lasers, nonlinear photonic devices such as soliton Kerr frequency combs or quantum photonic circuits.

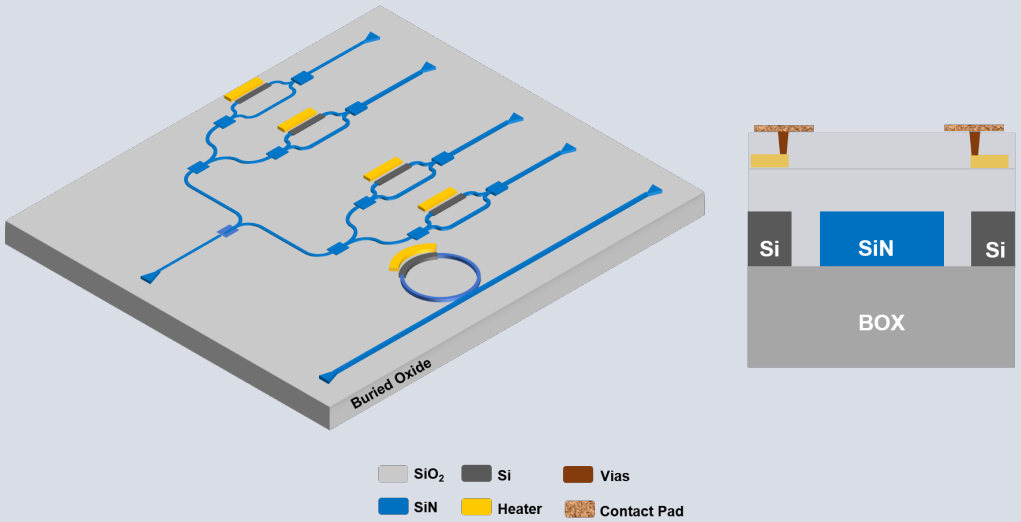


Damascene process flow for SiN Waveguide

SOI/SiN Hybrid Waveguide Technology

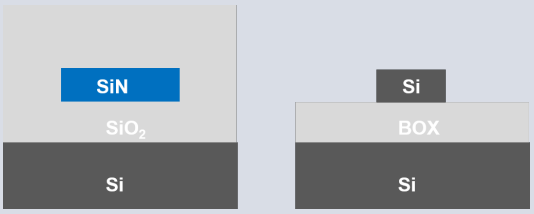
Associated Research Scholars: *Sarad S. Bhakat, Riddhi Goswami, Anushka Tiwari, Pranita Ku. Swain,*

The rapid development of fabrication techniques has boosted the resurgence of silicon-based Photonic Integrated Circuits (PICs). The silicon-on-insulator (SOI) and Silicon Nitride (SiN) platforms have been extremely successful in PIC development due to their CMOS compatibility. The devices are usually fabricated on a wafer following a planar process, where only one core material with a defined thickness is included. This traditional single-material platform cannot provide all the functionalities required for fully integrated PICs. By embedding thin-film SiN onto the SOI platform, SiN/Si hybrid photonic devices can be integrated on the same chip, simultaneously leveraging the advantages of both material platforms.



General scheme of SOI/SiN Hybrid photonic waveguide integration and cross-section.

Currently in PIC material technologies, no waveguide material can address the needs of all the potential applications of PICs. Therefore advanced PICs may require the best possible performance of a large number of different photonic elements in PICs to achieve the desired functionalities, which may not be possible with single waveguide material technology.



Different material platform for PICs

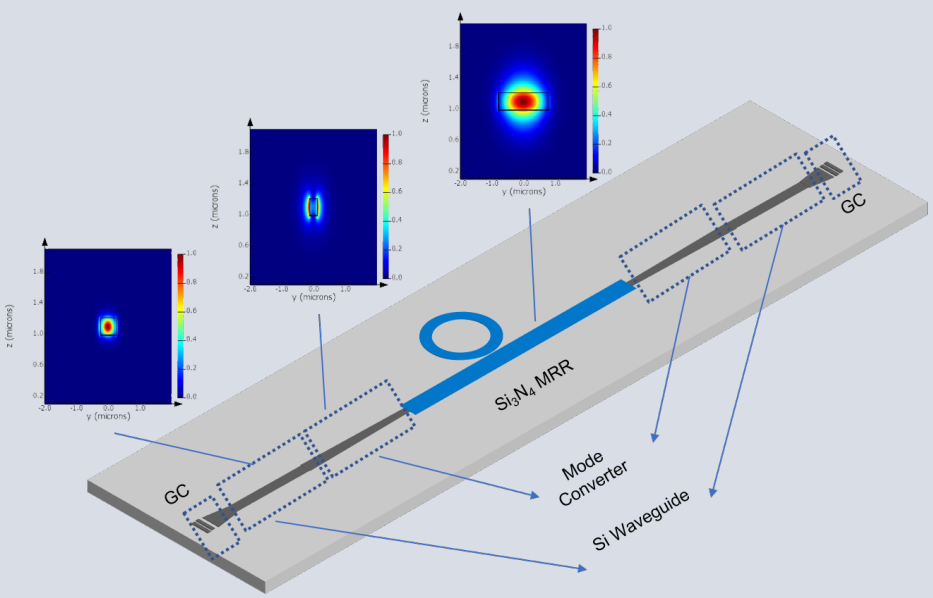
PIC Material Platforms at CoE-CPPICS

Below is a comparison between two waveguide material platforms, which are regularly used in our center to fabricate various photonic devices for different applications.

	Silicon Nitride	Silicon-on-Insulator
Wavelength range	0.3 µm – 3 µm	1.1 µm – 4.5 µm
Lasers, Amplifiers	NA	NA
Photodetectors	NA	++
Modulators	NA	+
Thermo-optic phase shifter	++	+++
Low-loss passive devices	+++	++
Fiber to chip coupling	+++	++
Packaging	+++	+++
Electronic-Photonic Co-integration	+++	+++

+++ : excellent, ++ : very good, + : good

Device Design



In-plane SiN/Si hybrid ring resonator

We have identified two significant application areas where in-plane SiN/Si hybrid integrated photonic devices can offer clear advantages over single platform-based devices. First benefit is that we can get high-speed modulators and photo-detector arrays, with the feasibility of fabricating these devices in Silicon-on-Insulator (SOI) which is the most widely accepted platform for high speed active modulation. Secondly,for passive components like routing waveguides and delay lines, SiN material offers lower loss. Thus these hybrid devices can play a crucial role in minimizing optical losses, promoting lower power consumption, and enabling the dense integration of Photonic Integrated Circuits (PICs).

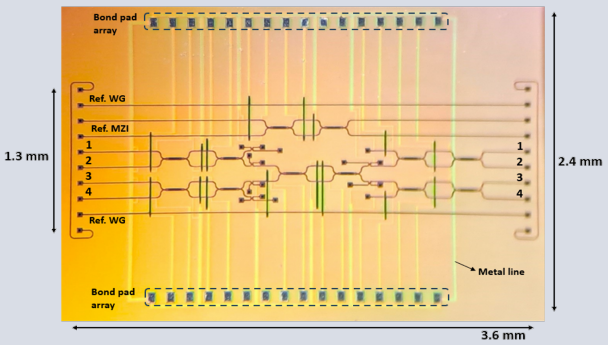
Photonic Circuits and Processors

Photonic circuits have diverse applications, spanning from Programmable Photonics, featuring versatile photonic processors, to Microwave Photonics, incorporating RF filters and optoelectronic oscillators. They also find applications in Quantum Integrated processors, which utilize photon sources, Quantum random number generators, Quantum key distribution, and Quantum processors.

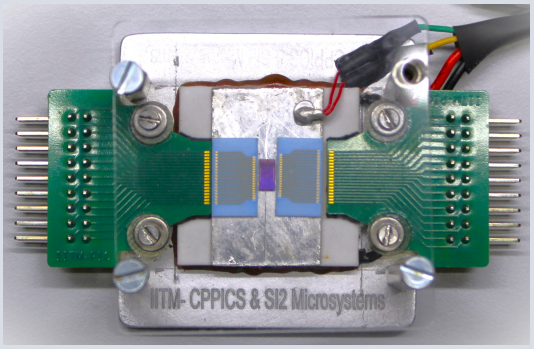
Programmable Photonic Integrated Circuits

Associated Research Scholars: *Kumar Piyush, Yash Raj, Akash Shekhar*

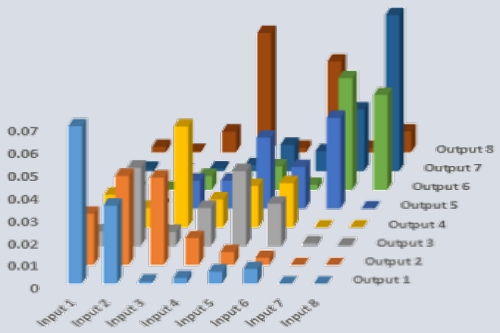
Silicon Photonics allows various ways to actively control(or program) the behavior of photonic devices using external stimuli like electrical signals, and local temperature changes to name a few. Using these ways, Programmable Photonic Integrated Circuits (PPICs) offer an efficient path for rapid prototyping, supplying a multifunctional, upgradeable, and software-defined platform for prototypes. Programmable photonics plays a cruicial role in diverse cutting-edge areas, including **hardware accelerators, autonomous driving, neuromorphic computing, quantum technology, avionics, and advanced communication, such as 5G and beyond.**



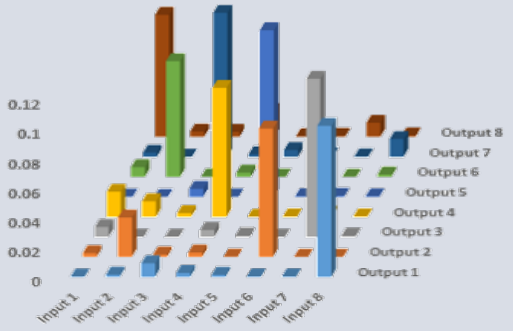
4x4 MZI feedforward architecture fabricated at IMEC 2023



IMEC chip packaged at Si2 Microsytems

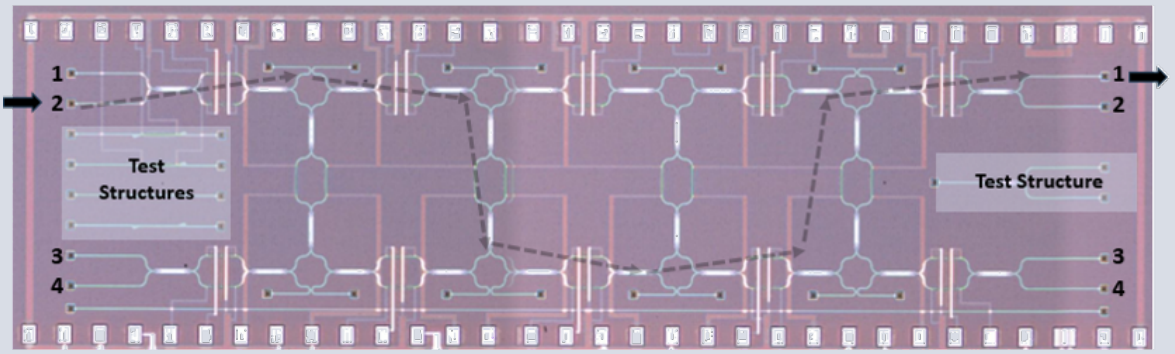


8x8 MZI Transmission with hardware errors



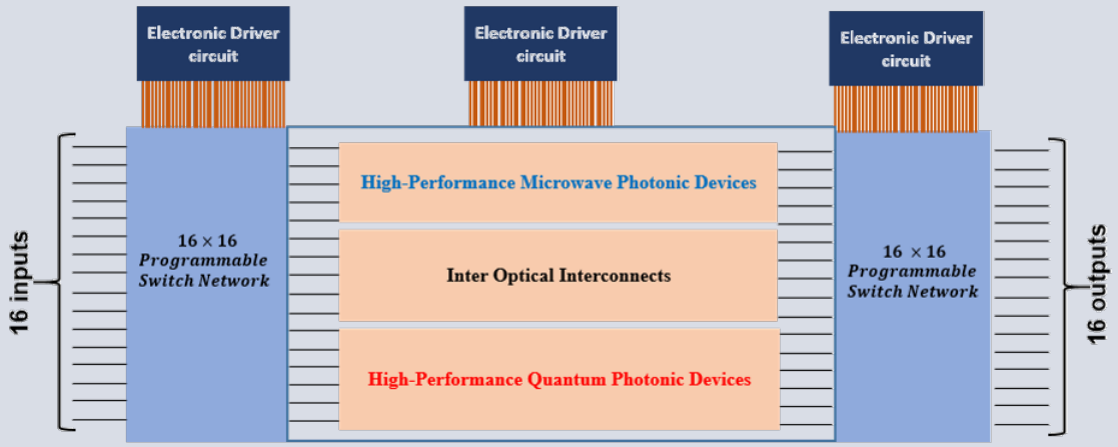
8x8 MZI Transmission after correction of hardware errors using local heaters

A major obstacle in advancing the widespread adoption of programmable photonics chips revolves around the availability of robust software support and design tools tailored for programmable photonics hardware. Within our group, we are currently working on the fabrication-induced hardware error correction for MZI mesh architecture which can be programmed for different output given for the same set of inputs.



4x4 square mesh, fabricated at IMEC. Arrow showing the path followed by light input at port 2 to output at port 1.

The future of programmable photonics shows great promise, particularly in emerging fields like neuromorphic computing and computing accelerators. Neuromorphic computing seeks efficient hardware and algorithms for tasks like pattern recognition and decision-making. Programmable photonics also offers substantial potential in high-performance computing and specialized computing accelerators designed to boost specific computational tasks. Integrating specialized high-performance photonic blocks within a central hub streamlines the incorporation of one or multiple modules. This central hub, featuring an NxN input and output switch, directed by external electronic drivers, transforms into a dynamic and versatile Multipurpose Programmable Photonic Processor, catering to a wide array of functions and applications.

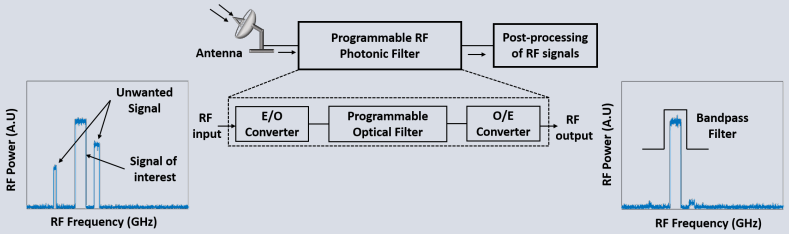


Multipurpose Programmable Photonic Processsor

Programmable RF Photonic Filters

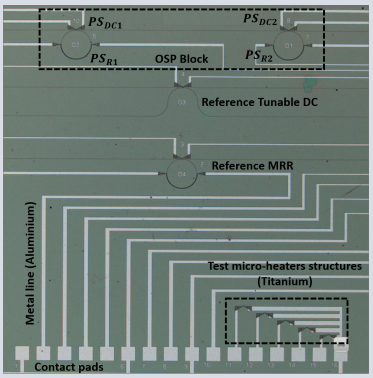
Associated Research Scholar: *Ashitosh Velamuri*

An RF filter is the basic component of any RF receiver architecture to separate the unwanted signal from the signal of interest. For this purpose, passive electrical filters are most commonly used because of their robustness and cost-effectiveness. However, these filters are designed to operate at a single frequency band with little to no scope for tuning and usually are power hungry especially at mmWave frequencies. The programmable RF photonic filters shows promise in terms of size, weight and power (SWaP), wide-band tunability and scalability, which are very crucial in 5G/6G and satellite communications and avionic applications.

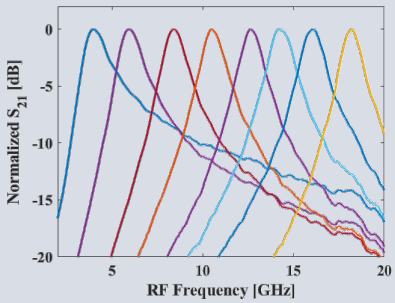


General scheme of RF receiver, emphasizing the RF filter functionality.

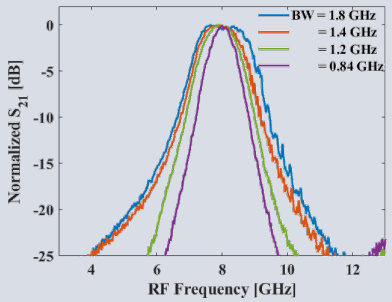
At CoE-CPPICS, we are working towards the developement of a working prototype of a widely tunable (beyond 40 GHz) RF photonic filter. We have proposed a novel operational scheme of the programmable optical filter to realize a tunable RF photonic filter with improved shape factor. The programmable optical filter was fabricated using the in-house fabrication facilities of Centre for NEMS and Nanophotonics (CNNP), IIT Madras. An RF filter which covers C, X and Ku bands (4-18 GHz) with a tunable bandwidth of 0.84-1.8 GHz was demonstrated. The RF-to-RF insertion loss of the filter is $\sim$ 0 dB across the tuning range for our experimental setup.



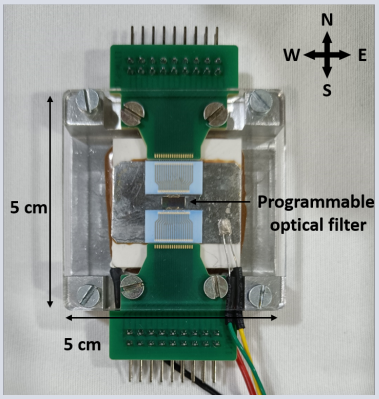
Programmable optical filter fabricated at CNNP, IIT Madras.



Tunable RF filter over C, X and Ku bands. Bandwidth = 840 MHz, insertion loss $\sim$ 0 dB



RF filter with tunable bandwidth (0.84-1.8 GHz) at 8 GHz.

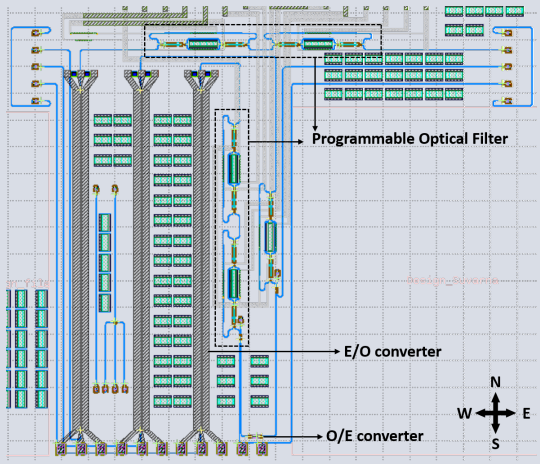


Beta version of the RF photonic filter prototype. Packaged at Si2 Microsystems, Bengaluru

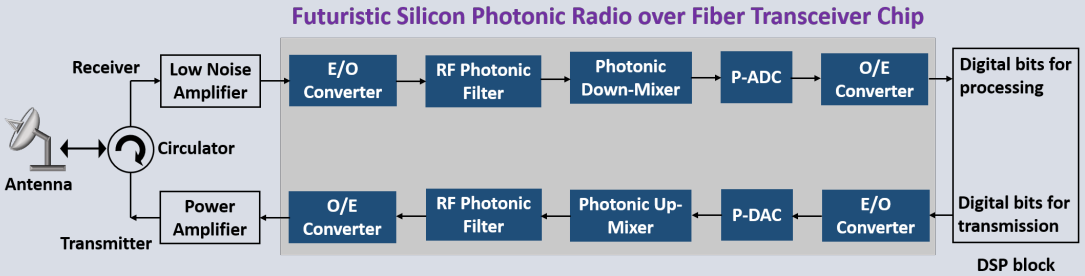
Packaging of a photonic integrated circuits is very critical step towards the prototype development/commercialization for different applications. Therefore, we have developed the packaging design rules for a photonic integrated circuit in collaboration with our industry partner Si2 Microsystems, Bengaluru, with optical I/O in east-west direction, DC connectors in the north and RF connectors to the south. An electrically packaged programmable optical filter with DC connectors in north and south was developed as the beta version of the programmable RF photonic filter prototype.

For the demonstration of the working prototype of an RF photonic filter, the design of an E/O converter, programmable optical filter, and O/E converter integrated on the same chip is taped out to IMEC Belgium. The RF filter prototype is expected to cover C, X, Ku and Ka bands with tunable bandwidth and negligible insertion loss.

At CoE-CPPICS, we believe that the full potential of the silicon photonic chip for microwave applications can be realized by implementing each of the RF processing blocks such as RF filtering, up and down-conversion of the data from/to the baseband, RF analog to digital and digital to analog conversion in the photonic domain. Bringing these microwave photonics RF processing blocks on a single chip will make the futuristic Radio over over-fiber transceiver systems.



Working prototype design of RF photonic filter design, taped-out to IMEC Belgium.

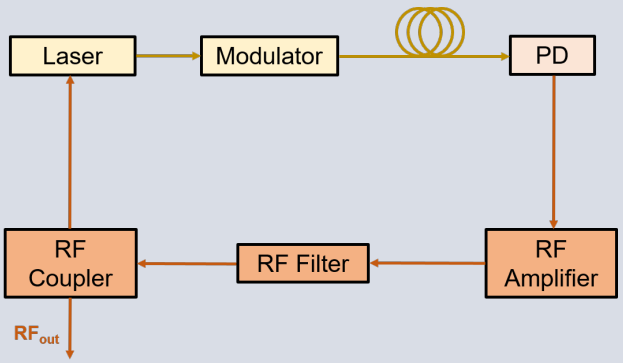


Schematic representation of the futuristic silicon photonic chip as a Radio over Fiber Transceiver

Photonic Chip based Optoelectronic Oscillator

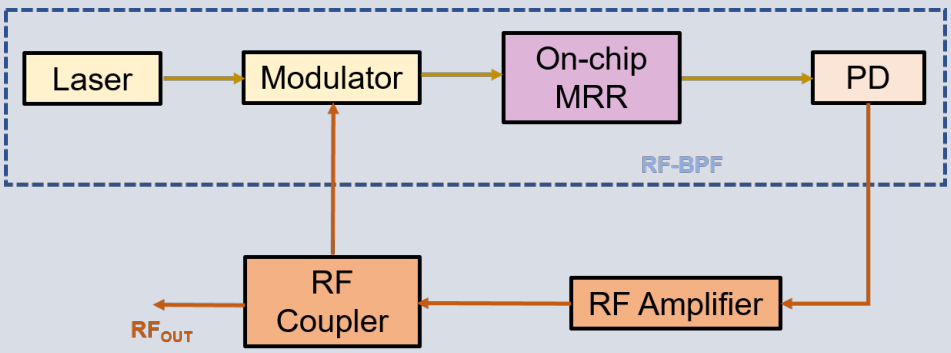
Associated Research Scholars: *Anushka Tiwari, Ashitosh Velamuri*

RF signal generation with low linewidth and phase noise is required in multiple applications such as radar systems, satellite communication and RF signal processing. In bulk optics, this is achieved majorly by frequency multiplication or with longer length of low-loss delay lines. In the conventional approach of optoelectronic oscillator (OEO) using long length of fiber, optical signal gets modulated with the electrically filtered signal from the photodiode (PD) noise. The optical modulated signal pass through a low loss fiber and detected in PD. Then the recovered modulated signal from the PD is amplified and pass through a bandpass filter to select frequency of operation by suppressing other cavity modes. Selected frequency of operation from RF filter is fed back to the modulator and forms an opto-electronic cavity leading to self-sustained oscillations once the loop gain exceeds the total loss of the loop. However, these systems are bulky and sensitive to external perturbations, also longer length of fiber delay line results in a large number of closely spaced eigenmodes. To generate spectrally pure RF signal, narrow bandpass filter is required to select single oscillator mode which makes it hard to procure electrical filter with these critical specifications of narrowband and tunability.



Basic scheme of OEO

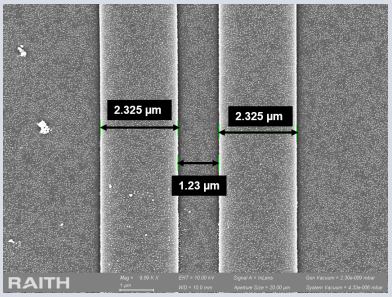
Recently, we have demonstrated the RF signal generation using microring resonator (MRR) on silicon nitride platform.



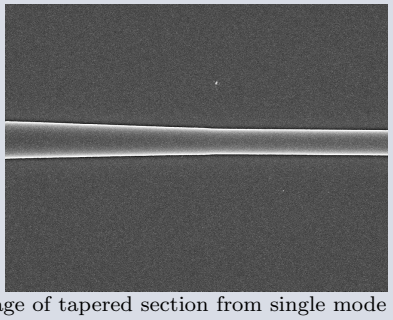
OEO scheme with integrated MRR

In this scheme, RF signal is generated and filtered in the optical domain from the transient RF noise and looped back in electrical domain to the modulator. The frequency of oscillation is decided from the difference between the laser wavelength (positioned near one of the resonances) and corresponding MRR resonance. One of the critical part of this scheme is to acquire narrow bandpass optical filter, for which low loss microring resonator with high quality factor could serve as evident solution.

Multimode configuration of MRR

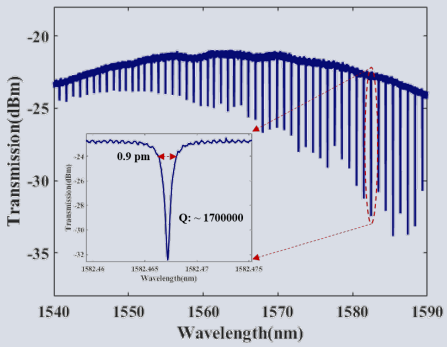


SEM image of DC section of multi-mode ring and bus waveguide

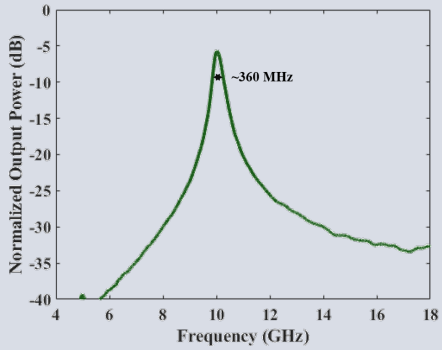


SEM image of tapered section from single mode to multi-mode waveguide

We have designed and fabricated multimode microring resonator using the in-house fabrication facilities of Centre for NEMS and Nanophotonics (CNNP), IIT Madras. Using multimode MRR, we could achieve the quality factor of $\simeq 1.7$ million.

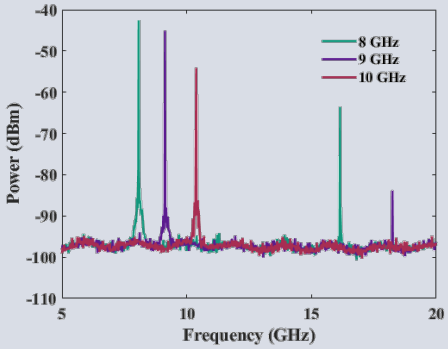


MRR response of ring radius 200 μm, inset: zoomed resonance with 3-dB bandwidth



Optical bandpass filter response using MRR

To demonstrate MRR based OEO we have used high quality factor MRR with multimode structure. Using the MRR in the scheme along with phase modulator, the optical link work as optical bandpass filter(BPF). Lower the filter bandwidth, lesser will be the selected cavity modes enhancing the phase noise of OEO cavity. Hence, with this design of the MRR we could achieve the BPF bandwidth of 360 MHz. Using same device we have demonstrated chip based OEO and generated RF signals with tunable frequencies where tunability is achieve by tuning the laser wavelength.

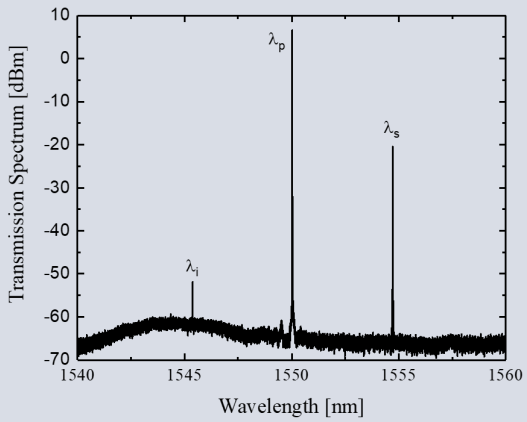


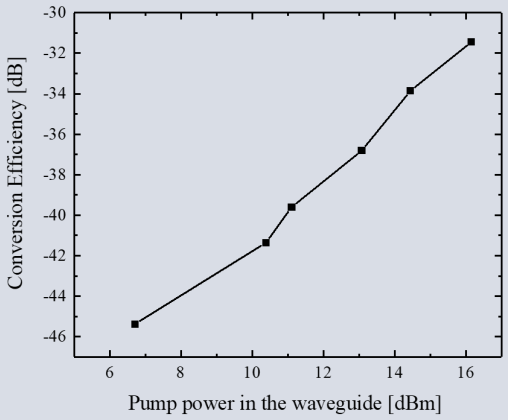
OEO generated signals with tunable RF frequency

Nonlinear Integrated Photonics

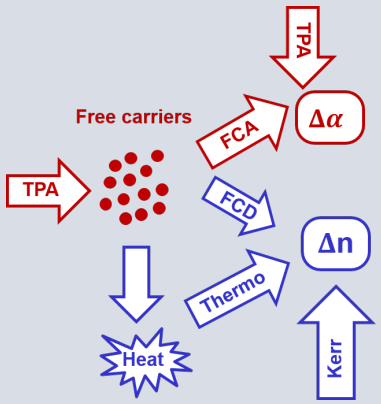
Associated Reserach Scholars: *Arnab Goswami, Anushka Tiwari, Pranita Ku. Swain, Nagarajan Nallusamy*

The distinctive attributes of nonlinear optical effects find practical utility within miniaturized photonic devices, enabling the manipulation of light in innovative and potent ways. CMOS-compatible integrated photonics holds significant promise across a spectrum of applications, including on-chip wavelength conversion, all-optical signal processing, parametric amplifiers, frequency combs, and photon pair generation. Our primary focus lies in utilizing four-wave mixing (FWM) for wavelength conversion in silicon and silicon nitride-based devices. Currently, we are actively engaged in research aimed at generating photon pairs and frequency combs within these integrated material platforms. The below figures illustrate the FWM spectrum and conversion efficiency in a 2 mm long silicon waveguide.





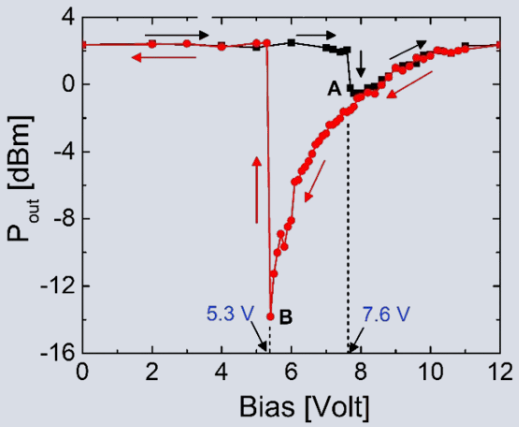
Compact microring resonator (MRR) with a suitably designed waveguide core in SOI substrate is an excellent device to enhance the field strength of a pump laser light for FWM based process. Nevertheless, optimizing silicon waveguides presents certain challenges, especially optical bistability due to self-phase modulation caused by the Kerr effect and mitigating the impact of two-photon absorption at communication wavelengths. This absorption subsequently leads to free carrier-induced plasma dispersion, making it crucial to address these issues to precisely control the strength of the pump field at resonance wavelengths with the phase shifter incorporated MRR.

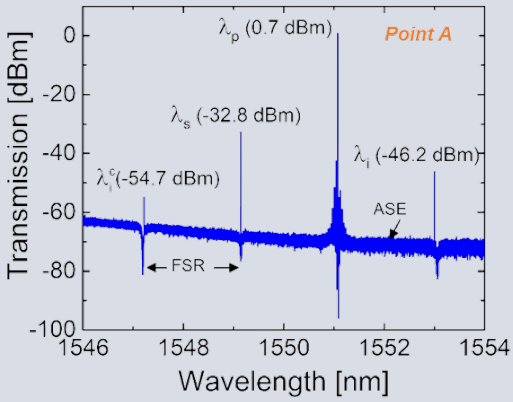


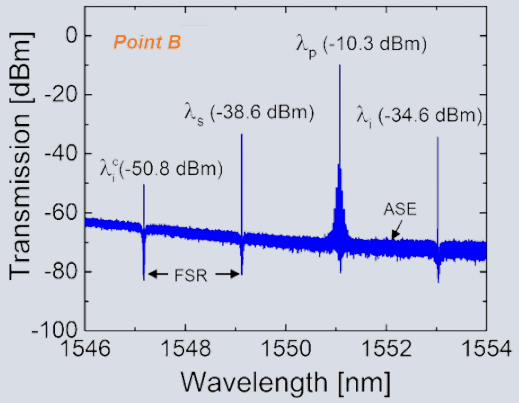
Non-linear mechanisms at high power in silicon

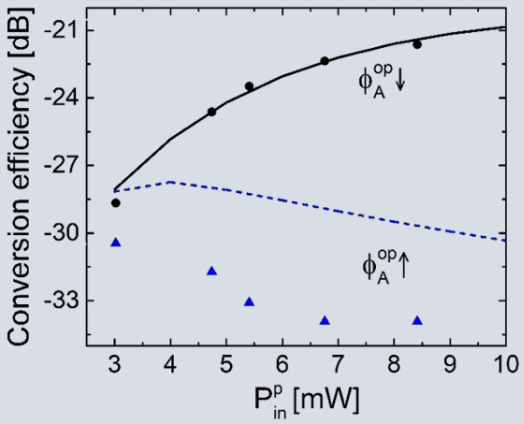
For a microring resonator of radius 50 μm, an improved stimulated FWM gain of $\sim$ 11.6 dB has been observed while thermo-optically blue-shifting resonances (point B) in comparison to that of

red-shifting resonances (point A), for a launched pump power of 8.4 mW operating at a slightly off-resonant wavelength λ_p.

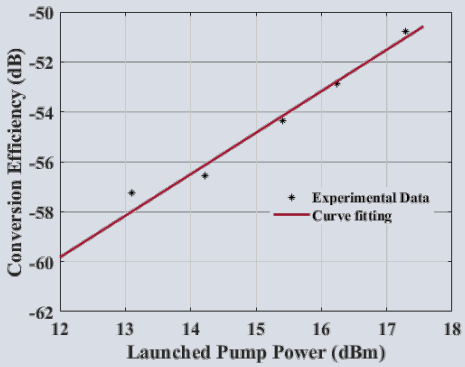








The combination of the absence of two-photon absorption (TPA) and minimal waveguide losses in silicon nitride-based waveguides equips them to withstand high optical powers without succumbing to the adverse effects of TPA. We have successfully demonstrated stimulated FWM in an in-house developed silicon nitride device with a device layer thickness of 400 nm and a device length of 2 mm. Besides, we are actively exploring its applications for photon pair generation, frequency comb generation and nonlinear optical processes, utilizing our in-house technology.



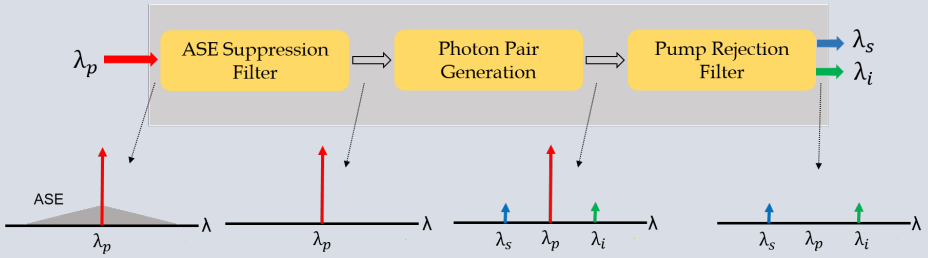
Conversion efficiency of FWM in SiN waveguide

Currently, our focus lies in generating frequency combs through the utilization of low-loss waveguide-based microring resonators. These combs offer a comprehensive spectrum of evenly spaced optical frequencies, thereby enabling precision measurements, spectroscopic applications, and the calibration of optical clocks.

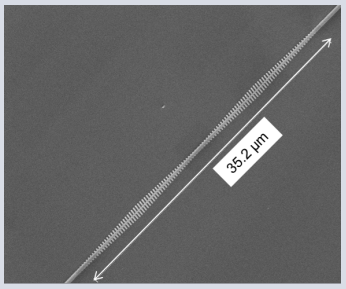
Quantum Photonic Sources

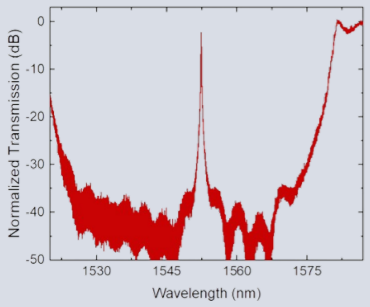
Associated Research Scholars: *Arnab Goswami, Pratyasha Priyadarshini, Ram Mohan Rao Boyapati*

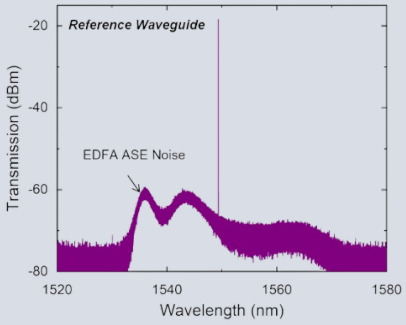
Photon pair generation through spontaneous four-wave mixing (FWM) in silicon waveguides or microring resonators stands as a pivotal requirement in the realm of large-scale integrated quantum photonics. Nonetheless, it is crucial to employ an amplified spontaneous emission (ASE) suppression filter to mitigate the introduction of noise within the photon pair generation band. Due to the inherent challenge of modest conversion efficiency, it is imperative to promptly filter or attenuate the surplus unused pump light by over 100 dB to avoid any noise to the originally created photon pairs along the path. Consequently, a fully integrated quantum photonic source necessitates the inclusion of both these filter types.

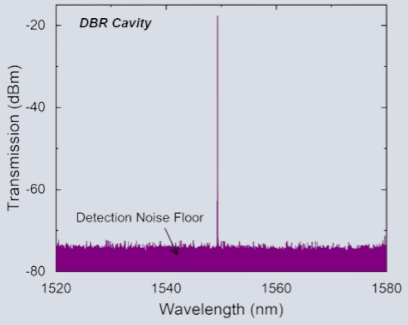


A design of compact DBR resonators ($\sim$ 40 μm-long) integrated into SOI rib waveguide structure has been demonstrated, exhibiting a resonance bandwidth as low as 40 pm ($\lambda_r \sim$ 1550 nm) with an extinction of $\sim$ 35 dB over a rejection band of $\sim$ 60 nm. The resonance peak has been thermo-optically tuned over a wide range of wavelength at a rate of 95 pm/mW. The device is shown to be effective in ASE noise suppression of an amplified pump laser.

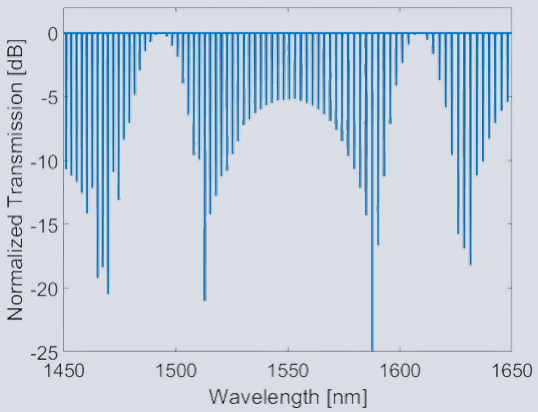


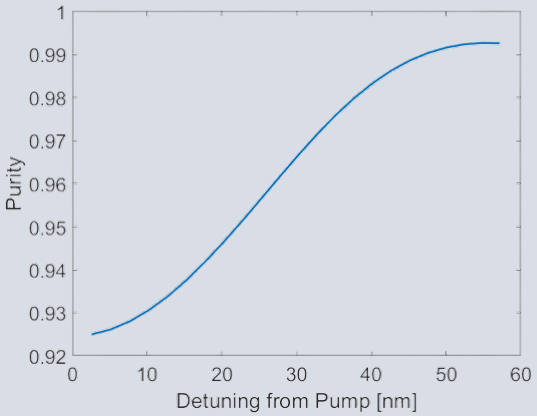




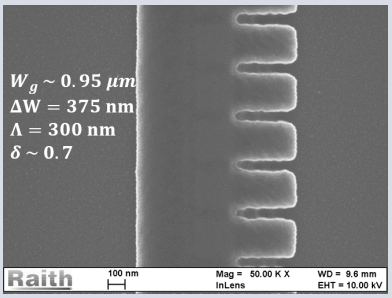


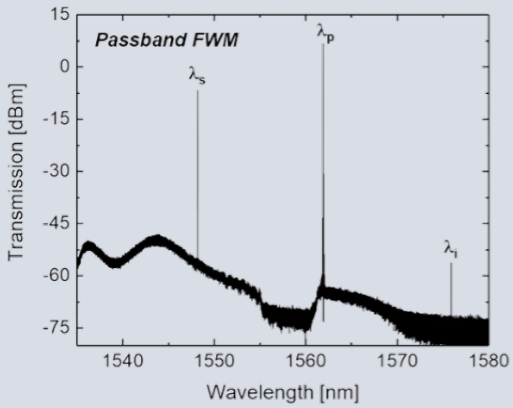
For single photon source, it is crucial, that these photon pairs remain entirely unentangled to produce heralded photons in spectrally pure states. This purity is instrumental in achieving high visibility in quantum interference. An MRR with a novel design of directional coupler can overcome the traditional purity limitation of $\sim 93\%$ and achieve purity up to $\sim 99\%$, depending on the choice of photon pairs around 1550 nm.

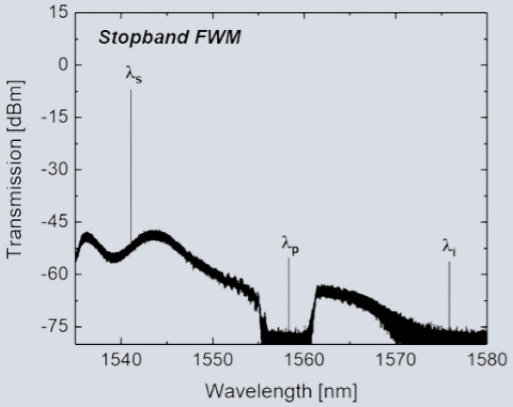




We have designed a DBR based stop-band filter around phase-matched Bragg wavelength of λ_B ∼1550 nm in a multimode rib waveguide section such that the photon pair source is protected from back reflected pump. We demonstrated on-chip pump rejection of $>$ 63 dB for stimulated four wave mixing experiment using a single stage DBR filter of length 450 μm.





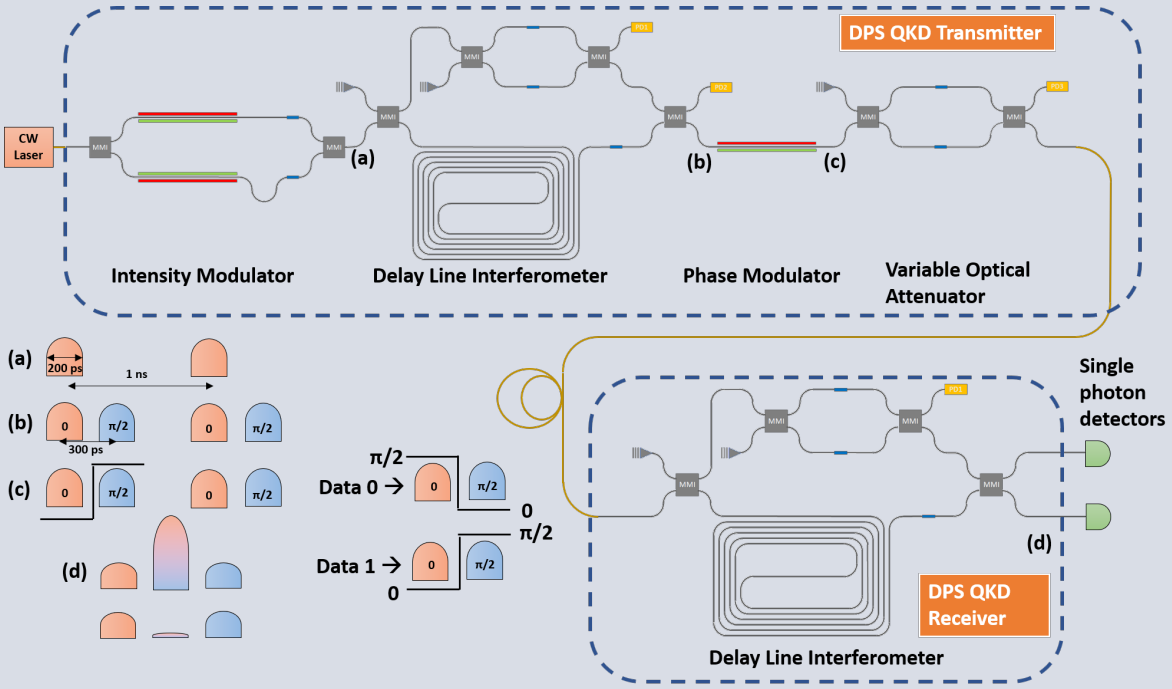


The integration of ASE filters, photon sources, and pump rejection filters represents a significant step toward realizing noise-free quantum photonic sources. The ongoing efforts to optimize photon pair generation rate, second-order coherence, and the accidental-to-coincidental ratio promise to bring us closer to the realization of advanced quantum technologies in a large-scale photonic integrated circuits.

Quantum Key Distribution Transceiver

Associated Research Scholars: *Ram Mohan Rao Boyapati, Suvarna Parvathy, Arnab Goswami, Yash Raj*

Classical cryptography depends on the time complexity of a mathematical problem such as the factorization of the product of two large prime numbers. But with the help of Shor's algorithm, quantum computers can solve the factorization problem in less time which is a huge threat to security. However, quantum key distribution uses quantum mechanics to ensure unconditional security. Practical implementation of QKD protocols based on bulk optics has been shown. Bulk optics-based QKD implementations occupy large space and also faces stability issues. Implementation of QKD on chip offers compact size, high stability, and robustness.

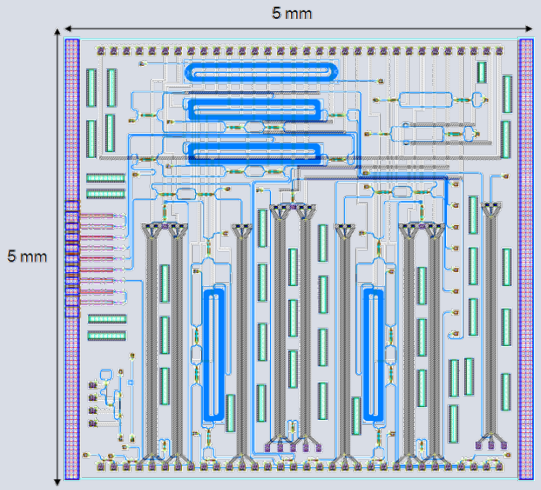


Design of DPS QKD on chip

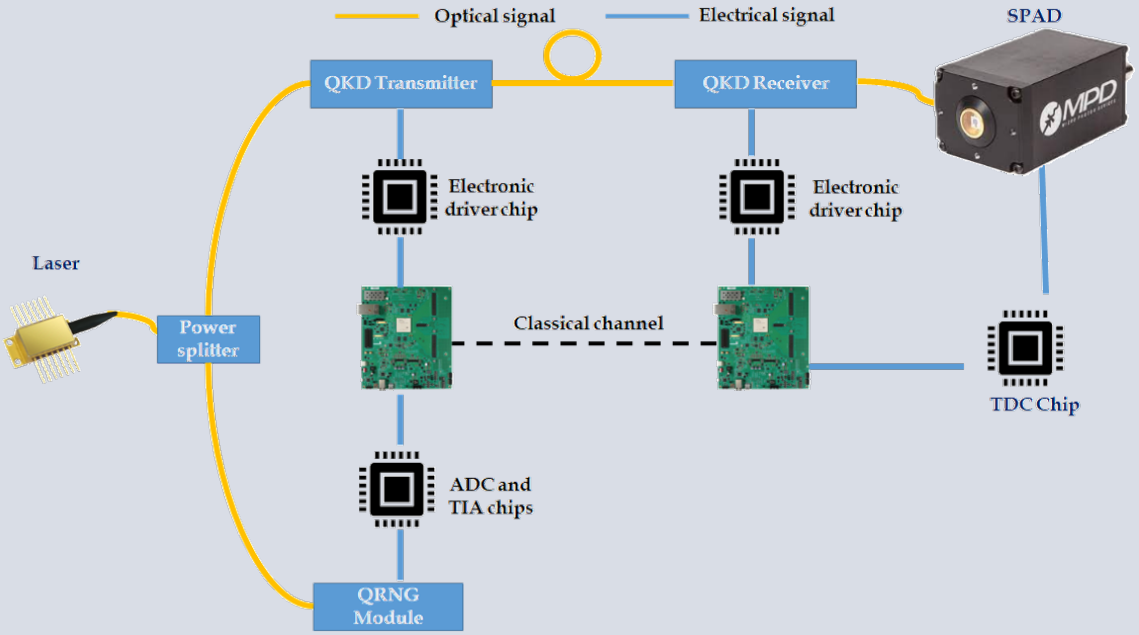
We have designed an on-chip Differential Phase Shift (DPS) QKD circuit and given it for tape-out. The information in the DPS QKD protocol is the phase difference between the two consecutive pulses. The continuous wave laser is launched into the chip using an edge coupler. The intensity modulator is used for making pulses of 200 ps pulse width and repetition rate of 1 ns. The pulses pass through the delay line interferometer to make two pulses with a delay of 300 ps and a phase difference of $\pi/2$. The MZI in the upper arm of the delay line interferometer is used as a variable optical attenuator to match the power of two pulses. The phase modulator is used for modulating information on the pulses depending on the data. If the data is zero the first pulse gets $\pi/2$ phase and the second pulse gets 0 phase whereas if the data is 1 the first pulse gets 0 phase and the second pulse gets $\pi/2$ phase. At the end, variable optical attenuator (VOA) is used to attenuate the pulses to a single photon level.

At the receiver side, similar DLI is used to extract the data by interference. There are three timewindows at the receiver i.e. the early timewindow, the interfering timewindow, and the late time window. The photon detection in early and late timestamps are discarded whereas in interfering timestamp, each of the single-photon detectors get clicked depending on the data. Once the receiver gets the data, the transmitter and the receiver do the error correction and privacy amplification to obtain the secure key.

We have submitted the design for tapeout in the IMEC ISIPP50G MPW run and currently awaiting the chip delivery. Both the transmitter and receiver are on the same chip making it as QKD transceiver.



Layout of DPS QKD transceiver taped-out of IMEC Belgium.



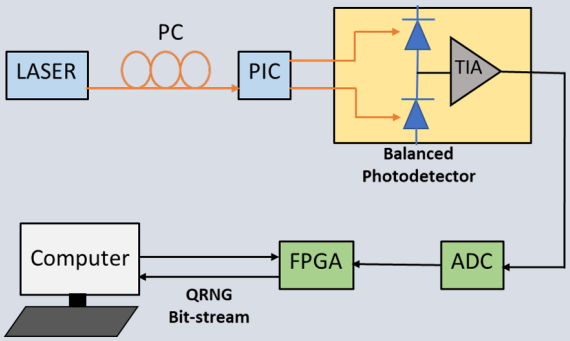
Compact QKD device with on-chip QKD transceiver and on-chip QRNG

Along with this transceiver chip at CPPICS IIT Madras, we want to demonstrate the compact QKD device with an on-chip QKD transceiver and on-chip QRNG with optically packaged and bringing the packaged electronic chips onto the same PCB board.

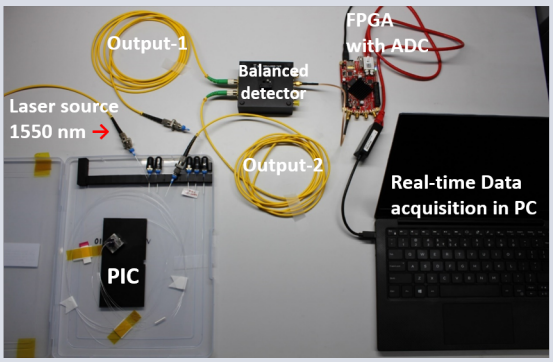
Quantum Random Number Generator

Associated Research Scholars: *Ankan Gayen, Adithya G S, Shamsul Hassan*

In daily life, knowingly or unknowingly, we are using different applications of random number generators. For example, one-time password (OTP), pins provided by the bank, CAPTCHAs etc. are the outputs of a random number generator. High-quality random numbers are needed to ensure security of these transactions/communications. Among different kinds of random numbers, Pseudo random Number and physical random numbers may be predicted by quantum computer, hence cannot be usable for the case of secured communication schemes, such as classical cryptography, or quantum key distribution (QKD) protocols followed in Quantum Communication. On the other hand, true random number generators (TRNGs) harness natural, stochastic random processes as the source of randomness, hence producing extremely high quality random sequences.

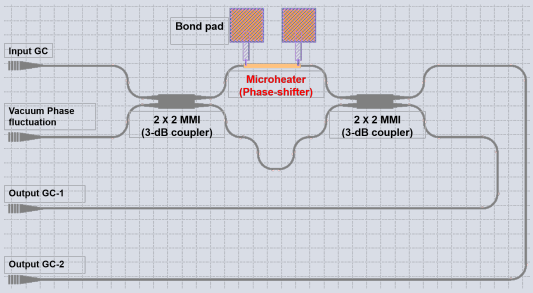


Block diagram of PIC based QRNG



Experimental realization of QRNG

Quantum Random Number Generator (QRNG) is a type of TRNG where the source of randomness is generated from quantum-mechanics driven physics. Among various sources of entropy that exist in quantum physics, the sources present in the field of optics is capable of generating random numbers at a very high speed. We have exploited the vacuum noise fluctuation as the source of randomness in our experiment. The experimental setup is shown above, where the same source of randomness is exploited to generate real-time truly random bit streams.

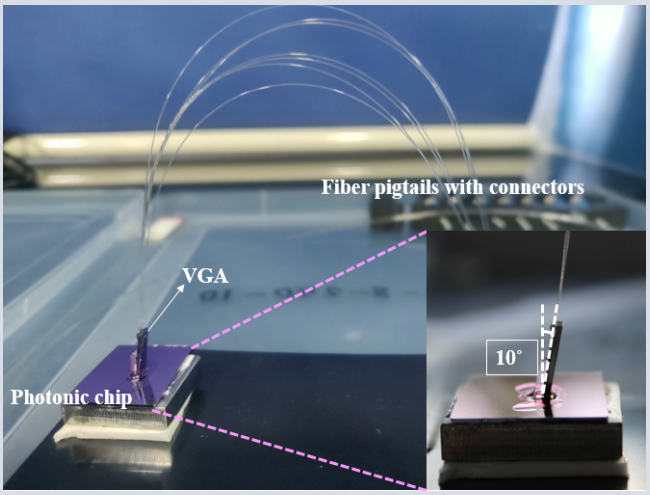


PIC design layout for QRNG

The PIC design layout for QRNG is shown in left figure. It is composed of MZI structure having MMI based 3-dB splitter and phase shifter at the arm of MZI. It can be fabricated by leveraging our in-house integrated silicon photonics technology and also compatible with CMOS fabrication foundries. The corresponding experimental set-up of PIC based QRNG is already illustrated above. From Laser source, light is launched into PIC through on-chip grating coupler and polarization controller (PC) is used to enhance the power coupling efficiency by controlling the TE/TM

polarization of the light. The output of PIC is given to a balanced homodyne detector with in-built Trans-Impedance Amplifier (TIA) to obtain shot noise signal by subtracting the classical noise. The analog-to-digital converter (ADC) is used for RF signal (analog signal) to digital signal conversion and post processing is performed by FPGA to generate real-time QRNG data.

The fiber-to-photonic chip attachment has been done to perform the QRNG experiment. Here, a special type of fiber array is used for fiber-to-chip light coupling, called V-Groove Array (VGA). There, all the fibers are equi-spaced, and the same pitch is maintained between the Grating Couplers (GCs) on chip, so that the alignment of the extreme two optical fibers with the corresponding GCs automatically ensures the alignent of the rests. After attaching the VGA to chip using an UV-curable index matching adhesive, the final look of the fiber attached QRNG chip is shown in the right figure.



Fiber attached QRNG chip

Our future plan is to integrate the photonic circuit and the balanced photodetector circuit in a monolithic CMOS compatible (SOI) platform. All the other required components for QRNG will be assembled on a single PCB board, that will drastically reduce the form factor of the module. We already demonstrated a TEC controlled and electrically packaged photonic chip which is discussed in details in the packaging section, thus proceeding towards a fully packaged Quantum Random Number Generator prototype.

Advantages of PIC-based QRNG

- Scalability (CMOS compatible platform)
- Low cost in mass production
- High generation rate
- High randomness due to vacuum phase fluctuation source of entropy
- High stability
- High flexibility (in terms of applications)

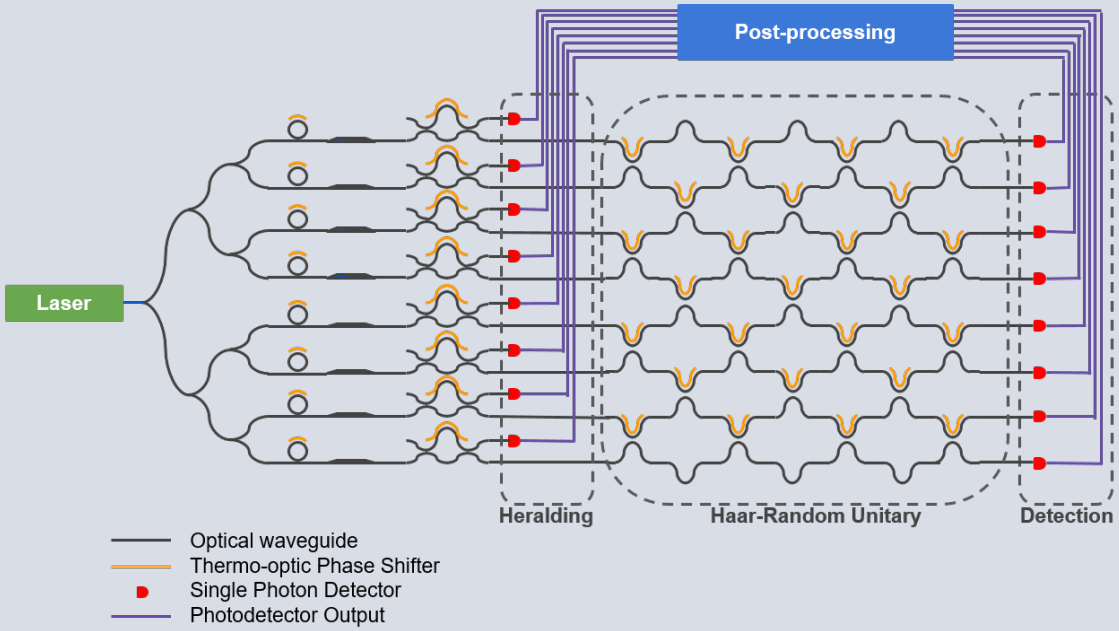
Applications

- Any cryptographic algorithms
- QKD transceiver
- Scientific Modelling & Simulations
- IT security for military and defence
- Financial transactions/ OTP/ Blockchain
- Gaming applications

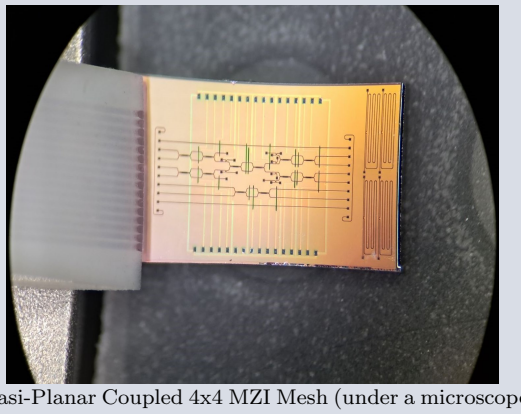
Quantum Photonic Computation

Associated Research Scholars: *Yash Raj, Ram Mohan Rao Boyapati, Arnab Goswami*

One of our main goals is to develop a scalable platform for quantum photonic computation. Silicon Photonics allows for the implementation of quantum photonic experiments in a very small footprint which ensures the phase stability of the system and makes the system more resilient to ambience fluctuations. We are working towards an efficient demonstration of the Boson Sampling experiment on the Silicon Photonic platform. Low-loss waveguides, high-quality indistinguishable photon sources, phase-stable interferometric circuits, and high-efficiency photodetectors are key ingredients to successfully realize this experiment.



Scattershot Boson Sampling



Quasi-Planar Coupled 4x4 MZI Mesh (under a microscope)

A 2x2 Mach-Zehnder Interferometer (MZI) with a Phase-Shifter in one of the input or output ports and the arm(s) to introduce arm imbalance can perform a universal unitary operation on two spatial mode light inputs, serving as a basic building block in an NxN MZI architecture. Such an interferometric circuit is important in the transformation of multi-spatial-mode photon states. We recently taped out a 4x4 MZI mesh for applications including Boson Sampling from IMEC, Belgium.

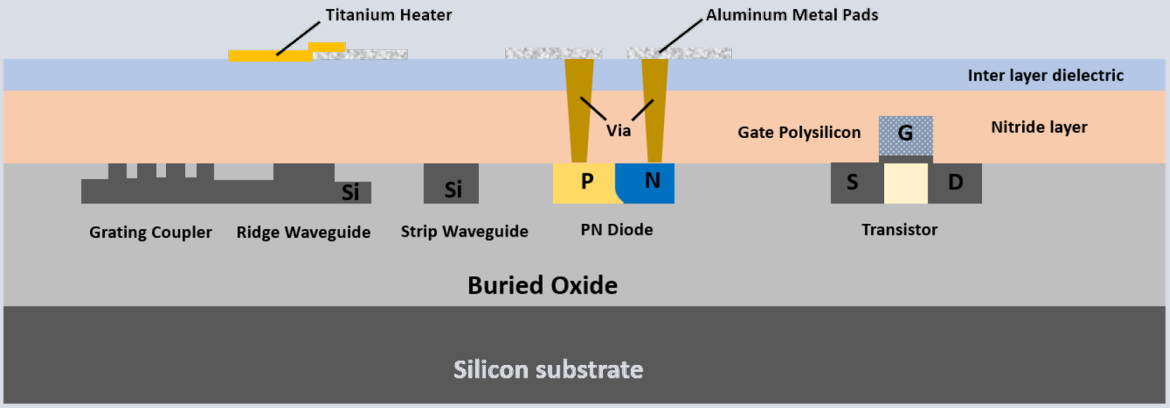
Silicon Photonics System Integration

Photonic system integration combines photonic, electronic, and thermal components of a photonic integrated circuits (PICs) using electronic-photonic co-integration and packaging. Silicon photonics integration is vital for incorporating PICs into products like optical transceivers, LiDAR systems, and optical sensors.

Electronic Photonic Co-Integration

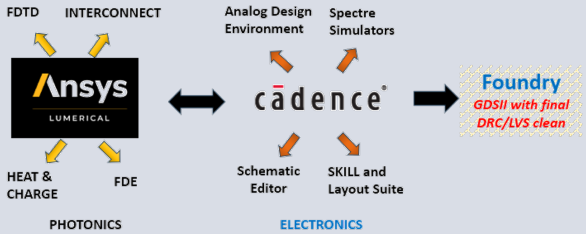
Associated Research Scholars: *Kumar Piyush, Lokesh Gajbhiye, Akash Shekhar, Ram Mohan, Suvarna Parvathy, Pawan Kumar*

Photonic system integration unites two vital technologies: electronics and photonics, merging their strengths into a single chip. Electronics can handle computational tasks efficiently but there is lag in speed and energy efficiency over long distances. Photonics, in contrast, beams data at light speed with minimal energy use. This fusion meets the need for faster, more efficient data transmission, slashing latency and interference risks. In applications like **data centers**, **telecommunications**, and **quantum computing**, where data demands are surging, electronic-photonic integration bridges the gap and unlocks the unique advantages of both technologies.



SOI CMOS process cross-section with both electronics and photonics component

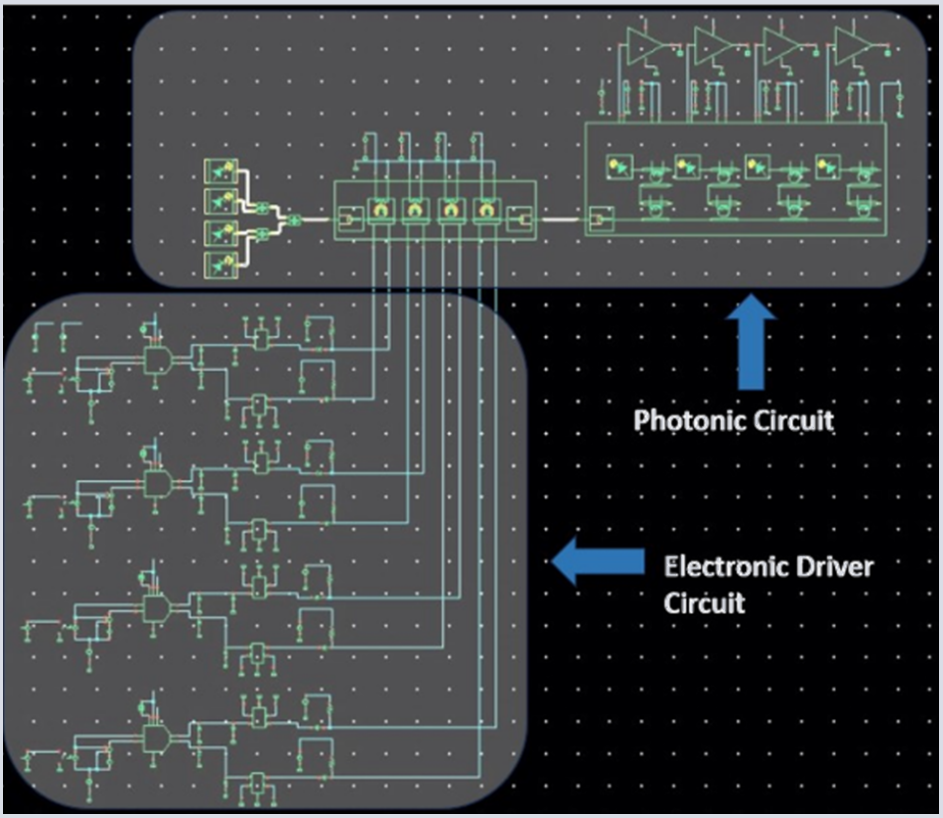
Electronic-Photonic Co-Design Platform: To assess the enhanced functionality co-integration, a co-simulation platform is vital. It requires the existing EDA tools to support photonic schematics, ensuring clear separation of optical and electrical connections to prevent inadvertent crossovers. The Electronic Photonic Design Automation **(EPDA)** framework helps designers in schematic capture, circuit simulation, schematic-driven layout and extends support to intricate photonic p-cells as well as advanced photonic layout generators.



EPDA Environment

Electronic-Photonic Co-Packaging techniques: The shift from electronic-photonic blueprints to actual production hinges on advancing fabrication and packaging methods that blend electronic and photonic elements. Diverse co-packaging techniques are there, including **Side-by-side wire bonding, 2.5D integration on an interposer, flip chip/micro pillar integration, 3-D stacking with through silicon vias, and monolithic integration.** Monolithic integration condenses everything onto a single chip but complicates design and thermal control. Flip chip bonding resolves some of these challenges but may encounter electrical and thermal interference.

At IITM, we are actively involved in both co-design and co-packaging for electronic-photonic integration. In co-design, we are focusing on electronic driver design for photonic integrated circuits, utilizing technologies like TSMC 65nm, 28nm, and recently, we have also signed an NDA partnership with GlobalFoundries for 45nm SPCLO PDK which opens the path for the monolithic electronic-photonic design fabrication. Regarding co-packaging, we're collaborating with Si2 Microsystems and have also developed in-house photonic packaging capabilities.



Co-simulation of electronic and photonic devices in cadence photonics tool. The electronic circuit (at the bottom) drives the photonic circuit (at the top).

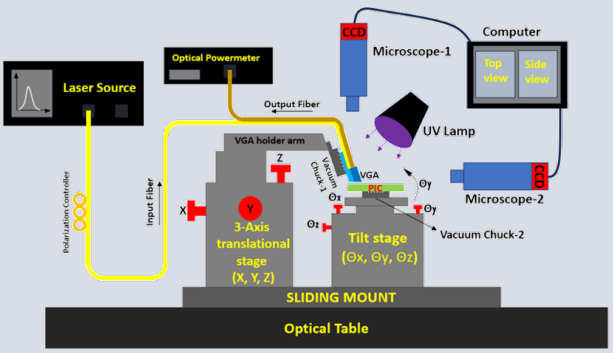
Fiber-to-Chip Attachment and Packaging

Associated Research Scholars: *Goutham Ezhilarasu, Nagrajan Nallusamy, Ankan Gayen, Shamsul Hassan, Vinoth Subramanian*

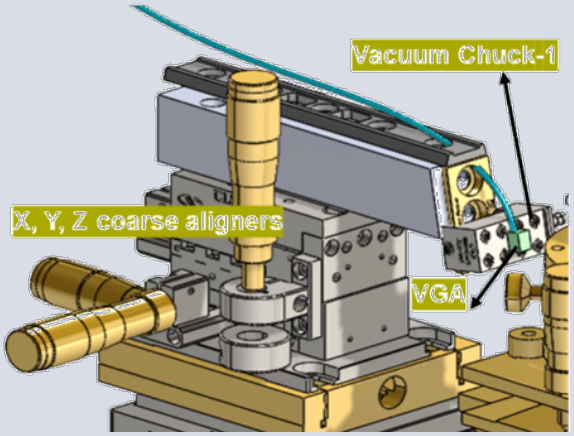
Integrated photonic components, commonly known as PICs, are manufactured using conventional semiconductor fabrication technologies and are hence highly cost effective at high manufacturing volumes with extremely small form factors. Even though such ground breaking benefits of PICs exist, their commercialization and widespread use have a major bottleneck: packaging & interfacing. Today, 70-80% of the cost of a photonic integrated module comes from the packaging and assembly process. This high cost comes due to the sophisticated manufacturing techniques that are needed to: Optically interface to the PIC, thermally manage the PIC to ensure strict temperature control and the large variety of packaging technologies that are to be simultaneously used for assembly. At CPPICS, we strive to address each one of these technology challenges to enable cost effective, efficient photonic integrated modules for information technological applications in India and the world at large.

Optical Interfacing

Optical interfacing to the PIC involves coupling the light directly from an optic fiber or an array of fibers into the photonic integrated circuit on the substrate. This can be done through the use of a grating coupler with an angled fiber (or array) or an edge coupling to a polished waveguide facet with a lensed fiber (or array). The precise alignment of the optical fiber, in each case, with the optical coupling structure on the PIC to ensure maximum mode field overlap and hence coupling is quite complex, expensive & time consuming. This is due to the fact that tolerances are limited and a 6-axis (X, Y, Z, tilt, roll, yaw) alignment is needed. In fact, for a grating coupler, tolerances are around a few microns while for an edge coupler, it can be less than 1 micron for ensuring precise mode field overlap. For the first time in India, we have developed this optical coupling technology in-house with the capability to perform single fiber, V-groove array (VGA), and Quasi-planar coupling (QPC) fiber array using the same universal setup as shown in the figure. As shown in the figure, the setup consists of: A 3-axis (X,Y,Z) micro-positioner with a fiber holder consisting of an extended arm and vacuum chuck for aligning the fiber (or array); A 3-axis tilt ($\theta_x, \theta_y, \theta_z$) micro-positioner with vacuum chuck for sample alignment.



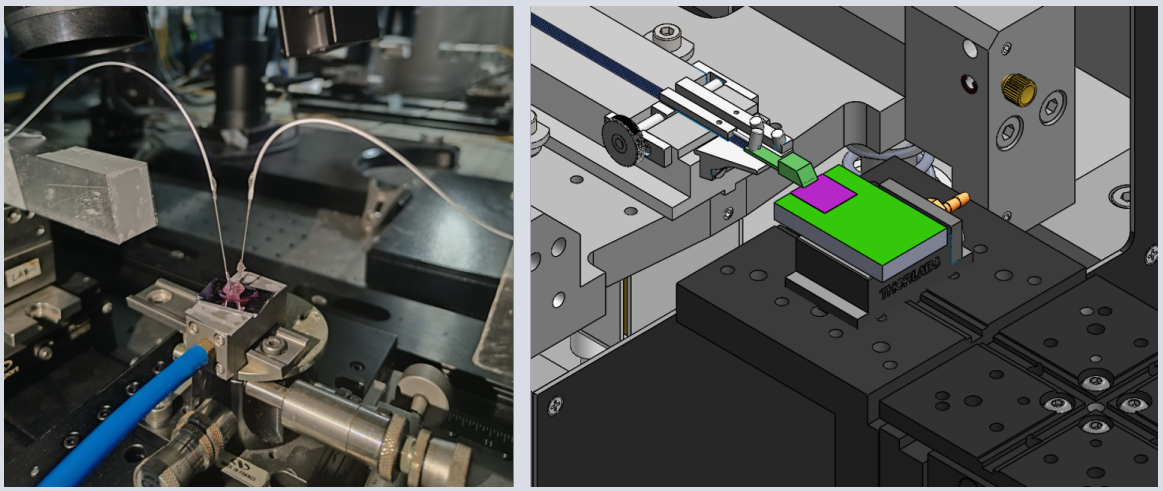
Optical coupling setup



Fiber alignment setup with 6-axis micro-positioner

Thermal Co-design

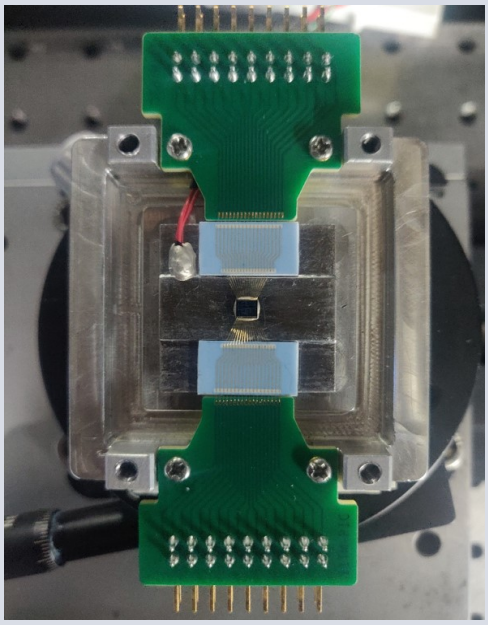
Photonic integrated circuits are highly temperature sensitive as even a slight shift in the effective refractive index of the photonic components due to a temperature change (Thermo-optic effect) can lead to a drastic change in its transmission spectrum. It is hence imperative to maintain the temperature of the PIC within fixed tolerance limits. Thermal design of the photonics module must take into account the heat generated within the PIC itself, due to on-board resistive heaters, as well as thermal crosstalk with other electronic ICs that are integrated as part of the system/module. The temperature control is hence done actively with a Thermo-Electric-Cooler (TEC) module and closed loop PID. Proper 'temperature-aware' placement of the various components, design of the heat sink, choice of materials & full system thermal modelling is hence to be done. Using state of the art thermal simulation tools available at CPPICS, such a design is possible. An example case where a single fiber attachment to the PIC is successfully performed along with proper thermal design is shown in the figure. Here, optical signals can be sent into the PIC through the input fiber and the output can be taken to a photodetector through the output fiber. The mechanical strength of the fiber attachment was verified through manual shear tests.



Single fiber attachment and schematic diagram of QPC coupling

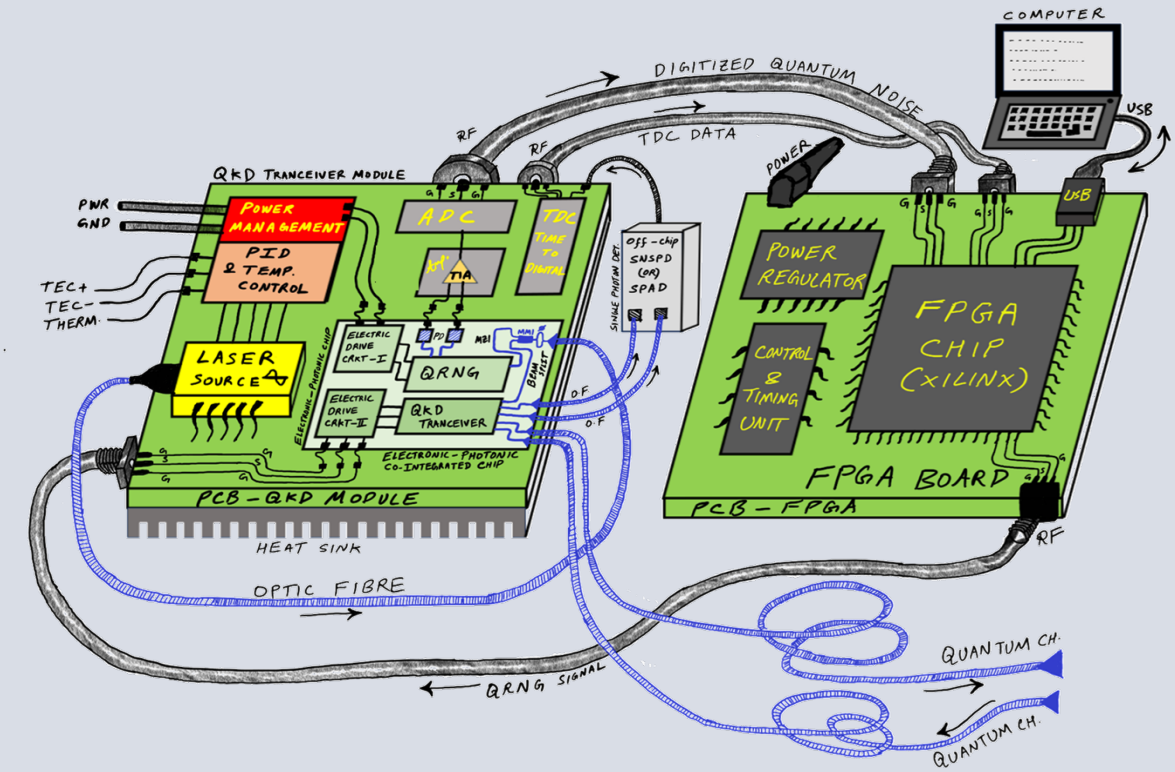
System Integration

At CPPICS, we aspire to streamline the entire photonic-integrated module design flow from the design & optimization of the PIC; optimal optical coupling to the PIC; design of electronic components on PCB; heterogeneous integration of the PIC, electronics, laser source & TEC; and the full system packaging with testing. We also work closely with out industrial partner, Si2 Microsystems, Bangalore to co-develop this infrastructure in India which will be one of a kind and serves to bring the state of the art in photonics & information technology to home turf. This will have a tremendous impact on the commercial and defense sectors. An example fully packaged demonstration of a PIC chip developed in collaboration with Si2 Microsystems is shown in the figure on next page. The package consists of a PIC mounted on a heat spreader attached to a TEC. The TEC is connected to the aluminum heat spreader as shown in figure. The PIC is wirebonded to the PCB for external connection to the control electronics. An external PID control can be used to stabilize the temperature of the package during operation.



Packaged PIC in collaboration with Si2 Microsystems

The figure below shows an example of a future chip based Quantum Key Distribution (QKD) module. As we can see, several components of different technologies are to be heterogeneously integrated together as part of the full system: PIC, EIC (Electronic Integrated Circuit), power modules, laser source, analog circuits like amplifiers, FPGA module, & TEC. The integration also involves the mixing and merging of different packaging & integration technologies: 6-axis alignment for optical coupling, wire bonding, solder bonding, adhesive attachment, etc. We hence find that photonic module design can be quite complex and requires the co-design of all the various components with their heterogeneous integration to meet the desired specifications. An important feature of such a heterogeneous/hybrid photonics package is the integration of all necessary optical components including an integrated laser source and photodetector as shown in the same figure.

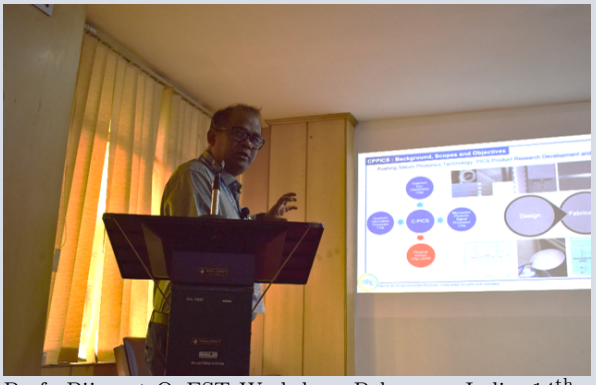


Schematic representation of our futuristic chip based QKD transceiver module

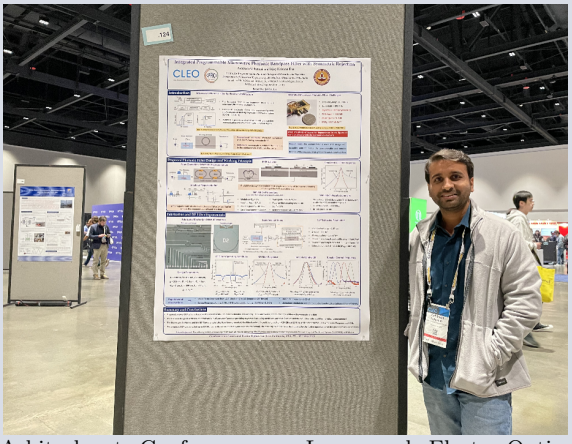
National and International Presence

Over the last two years, the research and development activities of our center of excellence have been presented and discussed at various national and international conferences, seminars, and workshops.

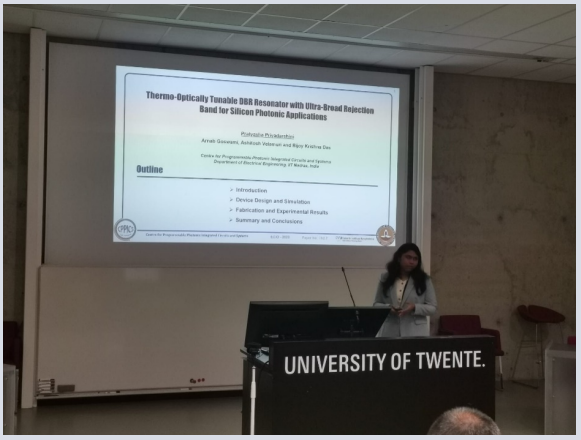
Anushka at 6th International Conference on Emerging Electronics (ICEE), Bangalore, India; 13th December 2022



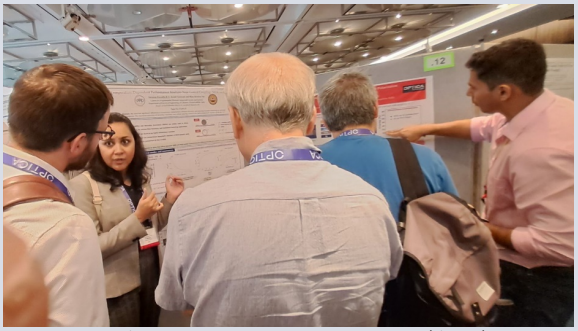
Prof. Bijoy at QuEST Workshop, Palampur, India; 14th May, 2023



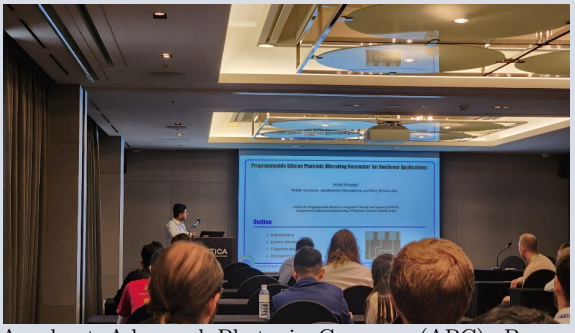
Ashitosh at Conference on Laser and Electro-Optics (CLEO), San Jose, California; 10th May, 2023



Pratyasha at European Conference on Integrated Optics (ECIO), Twente, Netherlands; 20th April, 2023



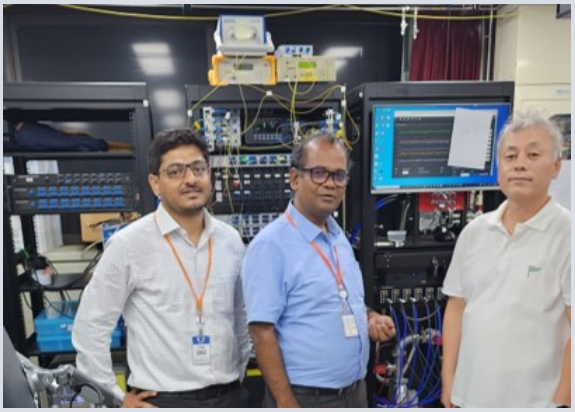
Suvarna at Advanced Photonic Congress (APC), Busan, South Korea; 11th July, 2023



Arnab at Advanced Photonic Congress (APC), Busan, South Korea; 13th July, 2023

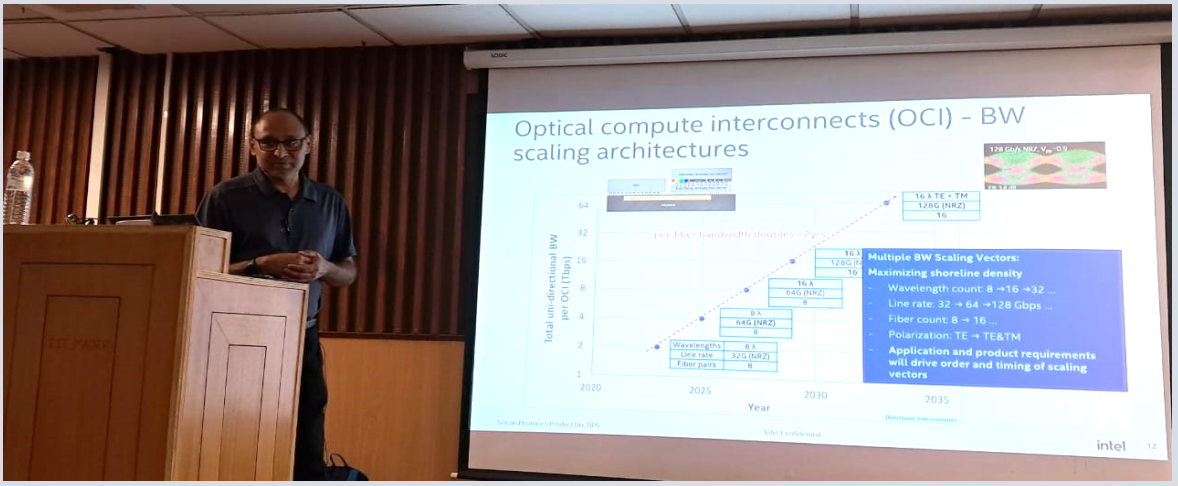
Dr. Mallik Tatipamula, CTO of Ericsson Silicon Valley during his visit to our Centre; 18th July, 2023

Mr. Kailash Narayan, President (Communications Group), Keysight Technologies at our lab; 21st April, 2023



Arnab and Prof. Bijoy at ETRI, Daejeon, South Korea with Dr, JongMoo Lee; 15th July, 2023

Conversation with Prof. Wim Bogearts at ICEE, Bangalore, India; 13th December 2022



Dr. Raghu Narayan, Principal Scientist in Silicon Photonics Division, Intel delivering a lecture at IITM on the Photonic Interconnects; 27th June, 2023

Visit of delegates (Niels Fache, Soumya Dey and Mohit Khanna) from Keysight at IIT Madras; 24th June, 2023

Our research scholars at the Workshop on Advances in Optical Communications organized at IITM Research Park; 23rd July, 2022

Our presence at Semicon India, Gandhinagar; 28th July, 2023

Lab outing with Industry Advisory Board Chairperson Dr.Mallik Tatipamula; 17th July, 2023

Ashitosh, Arnab, Dr. Sankha Dip Das and Prof. Bijoy at Digital India, Gandhinagar; 6th July, 2022

Prof. Bijoy and Arnab interacting with MeitY delegates (Dr. Sandip Chatterjee (Senior Director,MeitY), Smt. Sunita Verma (R & D Coordinator, MeitY) and Shri Alkesh Kumar Sharma (Ex. Secretary, MeitY)); 6th July, 2022

Smt. Sunita Verma (R & D Coordinator, MeitY) visiting our research facility; 20th October, 2022

Presenting Silterra 8 inch wafer to the honorable Union Minister of State for Communications, Shri Devusinh Chauhan at Workshop on Advances in Optical Communications, IITM Research Park; 23rd July, 2023

Publications

- Ashitosh Velamuri and Bijoy Krishna Das, "Programmable Silicon Photonic RF Filters with Symmetric Out-of-Band Rejection" IEEE Journal of Lightwave Technology, 2023.
- Suvarna Parvathy KV, Arnab Goswami and Bijoy Krishna Das, "Temperature Dependent Performance Analysis Near Critical Coupling: Microdisc versus Microring Resonators" Photonic Networks and Devices, Busan, South Korea, 2023.
- Arnab Goswami, Riddhi Goswami, Janakiraman Viraraghavan, and Bijoy K. Das, "Programmable Silicon Photonic Microring Resonator for Nonlinear Applications" Integrated Photonics Research, Silicon and Nanophotonics, Busan, South Korea, 2023.
- Pratyasha Priyadarshini, Arnab Goswami and Ashitosh Velamuri and Bijoy Krishna Das, "Thermo-optically Tunable DBR Resonator with Ultra-broad Rejection Band for Silicon Photonic Applications" European Conference on Integrated Optics, University of Twente, Netherlands, 2023.
- Ashitosh Velamuri and Bijoy Krishna Das, "Integrated Programmable Microwave Photonic Bandpass Filter with Symmetric Rejection" CLEO, San Jose, California, United States, 2023.
- Anushka Tiwari, Sarad Subhra Bhakat, Riddhi Goswami, and Pranita Kumari Swain, Arnab Goswami, Enakshi Bhattacharya and Bijoy Krishna Das, "In-house SiN process development for integrated photonic applications" ICEE, Bangalore, India, 2022.
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